SERVICE MANUAL FOR

8258I

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MiTAC

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MITAC 8258I portable notebook computer system.

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1.1.2 System Overview

The MITAC 8258I model is designed for Intel Mobile Pentium-M processor Yonah 533 and 667 FSB.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface. It also provides easy configuration through CMOS setup, which is built in system bios software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC/battery power indicator, battery charger indicator, HDD/ODD, NUM LOCK, CAP LOCK, Wireless LAN indicator. It also equipped with 10/100 LAN, 56 K fax modem, 4 USB ports, S-Video, audio Line-out/SPDIF, Line-in and internal/external microphone function.

The memory subsystem supports DDR2 SDRAM channels (64-bit wide).

The 945GM MCH host memory controller integrates a high performance host interface for Intel Yonah processor,

a high performance PCI Express interface, a high performance memory controller, and Direct Media Interface (DMI) connecting with Intel ICH7-M.

The Intel ICH7-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the audio controller with Azalia interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, the SATA controller and Direct Media Interface technology.

Intel graphics enhancements includes DVMT 3.0, Zone Rendering 2.0, Quad pixel pipe rendering engine, Pixel Shader 2.0 and 4x Faster Setup Engine.

The Realtek RTL8100CL is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI).

The ALC883 2-channel high definition audio codec with UAA (Universal Audio Architecture), featuring a 24-bit two-channel DAC and two stereo 20-bit ADCs, are designed for commercial notebook PC system. The ALC883 provides 2 output channels, along with flexible mixing, mute and fine gain control functions. Also, supporting 32-bit S/PDIF output functions and a sampling rate of up to 96 KHz.

The W83L951D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus

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mastering IDE, plug and play, Advanced Power Management (APM) with application restart, software-controlled Power shut-down.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	-Mobile Pentium-M Processor Yonah 533 and 667 FSB-Thermal spec 40W TDP
Core logic	Intel 945GM + ICH7-M chipset
System BIOS	SST49LF004A
Memory	DDR2 533 256 MB: Nanya, NT256T64UH4A1FN-37B Infineon, HYS64T32000HDL-3.7-B DDR2 533 512 MB: Nanya, NT512T64UH8A1FN-37B Infineon, HYS64T64020HDL-3.7-B
HDD	SATA : Fujitsu, MHV2040BH (Mercury60 series)
ODD	COMBO : Panasonic, UJDA770 or HLDS, GCC-4244N
Display	15.4" : AUO B154EW01 V8 None Glare Samsung LTN154X3-L01
Clock Generator	ICS 9LPR310
VGA Control	-Intel 945GM
LAN	RTL8100CL
Audio System	Azalia CODEC: ALC883
Modem	56 Kbps(V.90) Fax Modem (MDC (Azalia I/F)) Askey 1456VQL-R2
Wireless LAN	Wireless LAN Intel Pro/Wireless 3945ABG (Mini PCI-E Interface IEEE802.11a, b, g)
USB	USB2.0 x 4 (individual)
New Card	MINI-PCI-E interface

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1.2.1 Intel Yonah Processors in Micro-FCBGA Package

Intel Yonah Processors with 478 pins Micro-FCBGA package.

The Yonah processor is built on Intel's next generation 65 nanometer process technology. Yonah is Intel's first dual core processor for mobile.

The following list provides some of the key features on this processor:

- First dual core processor for mobile
- Supports Intel architecture with dynamic execution
- On-die, primary 32-KB instruction cache and 32-KB write back data cache
- On-die, 2 MB L2 cache with advanced transfer cache architecture
- Data prefetech logic
- Streaming SIMD Extension 2 (SSE2) and Streaming SIMD Extension 3 (SSE3)
- The Yonah standard voltage and low voltage processor are offered at 667 MHz FSB
- The Yonah ultra low voltage processor is offered at 533 MHz FSB
- Advanced power management features including enhanced Intel Speed-Step technology
- Digital temperature sensor

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- Micro-FCPGA and Micro-FCBGA package technologies
- Execute disable bit support for enhanced security
- Intel virtualization technology

1.2.2 Clock Generator

ICS9LPR310 is a low power CK410M-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. ICS9LPR310 is driven with a 14.318 MHz crystal.

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➢ Output Feathers

- 2 - 0.7 V differential CPU pairs
- 8 - 0.7 V differential PCIEX pairs
- 1 - 0.7 V differential SATA pair
- 1 - 0.7 V differential LCDCLK/PCIEX selectable pair
- 4 - PCI (33 MHz)
- 2 - PCICLK_F, (33 MHz) free-running
- 1 - USB, 48 MHz

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- 1 - DOT 96 MHz/27 MHz selectable pair
- 2 - REF, 14.318 MHz

➢ Key Specifications

- CPU outputs cycle-cycle jitter < 85 ps
- PCIEX outputs cycle-cycle jitter < 125 ps
- SATA outputs cycle-cycle jitter < 125 ps
- PCI outputs cycle-cycle jitter < 500 ps
- +/- 300 ppm frequency accuracy on CPU, PCIEX and SATA clocks
- +/- 100 ppm frequency accuracy on USB clocks

➢ Features/Benefits

- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318 MHz crystal, external crystal load
- PEREQ# pins to support PCIEX power management
- Low power differential clock outputs (no 50 ohm resistor to GND needed)

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1.2.3 The Mobile Intel 945GM Express Chipset

The Mobile Intel 945GM Express chipset is designed for use in Intel's next generation mobile platform code named NAPA.

The Intel 945GM Express chipset come with the generation 3.5 Intel integrated graphics engine, and the Intel Graphics Media Accelerator (GMA) 950, providing enhanced graphics support over the previous generation (G)MCH's.

The (G)MCH manages the flow of information between the four following primary interfaces:

- FSB
- System memory interface
- Graphics interface
- DMI

The (G)MCH can also be enabled to support external graphics, using the x16 PCI Express graphics attach port. When external graphics is enabled, the internal graphics port are inactive.

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Features:

- ➢ Processor Support
  - All Yonah variants

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- Merom support
- 533 MHz and 667 MHz Front Side Bus (FSB) support
- Source synchronous double-pumped (2x) address
- Source synchronous quad-pumped (4x) data
- Other key features are
  - Support for DBI (Data Bus Inversion)
  - Support for MSI (Message Signaled Interrupt)
  - 32-bit interface to address up to 4 GB of memory
  - A 12 deep In-Order queue to pipeline FSB commands
  - GTL+ bus driver with integrated GTL termination resistors

➢ Memory System

- Support single/dual channel DDR2 SDRAM
- Maximum memory supported 2 GB
- 64-bit wide per channel
- Three memory channel configurations supported
  - Single channel

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  - Dual channel symmetric
  - Dual channel asymmetric

- One SO-DIMM connector per channel
- Support for DDR2 at 400 MHz, 533 MHz and 667 MHz
- 256 Mb, 512 Mb and 1 Gb memory technologies supported
- Support for x8 and x16 devices
- Maximum memory supported: 2 GB
- Support for DDR2 On-Die Termination (ODT)
- Supports partial writes to memory using Data Mask signals (DM)
- Intel rapid memory power management
- Dynamic row power-down
- No support for fast chip select mode
- Support for 2N timings only

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- Internal Graphics
  - Intel Gen 3.5 integrated graphics engine
  - 250 MHz core rendor clock at 1.05 V core voltage
  - Supports TV-Out, LVDS, CRT and SDVO
  - Intel dual frequency graphics technology
  - Intel Dynamic Video Memory Technology (DVMT 3.0)
  - Intel smart 2D display technology
  - Intel display power saving technology 2.0
  - Video capture via x1 concurrent PCIE port
  - Higher performance MPEG-2 decoding
  - Hardware acceleration for VLD/iDCT
  - 4x pixel rate HWMC
  - DX 9.1
  - Hardware motion compensation
  - Intermediate Z in classic rendering

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- Analog CRT
  - Integrated 400 MHz RAMDAC
  - Analog monitor support up to QXGA (2048 x 1536)
  - Support for CRT hot plug
- Dual Channel LVDS
  - Panel support up to UXGA (1600 x 1200)
  - 25-112 MHz single/dual channel
    - Single channel LVDS interface support: 1 x 18 bpp
    - Dual channels LVDS interface support: 2 x 18 bpp panel support up to UXGA (1600 x 1200)
    - TFT panel type supported
  - Pixel Dithering for 18-bit TFT panel to emulate 24 bpp true color displays
  - Panel fitting, panning and center mode supported
  - CPIS 1.5 compliant
  - Spread spertrum clocking supported
  - Panel power sequencing support

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- Integrated PWM interface for LCD backlight inberter control

➢ TV-OUT

- Three integrated 10-bit DACS
- Macro Vision support
- Overscaling
- NTSC/PAL
- Component, S-Video and composite output interfaces
- HDTV support 480p/720p/1080i/1080p

➢ DMI

- Chip-to-chip interface between (G)MCH and Intel 82801GBM (ICH7-M)
- Configurable as x2 or x4 DMI lanes
- 2 GB/s (1 GB/s each direction) point-to-point interface to Intel 82801GBM
- 32-bit downstream address
- Direct Media Interface asynchronously coupled to core

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- Supports 3 virtual channels for traffic class performance differentiation
- Supports both snooped and non-snooped traffic
- Supports isochronous non-snooped traffic
- Supports legacy snooped isochronous traffic
- Supports the following traffic types to or from Intel 82801GBM
- Peer write traffic between DMI and PCI Express graphics port
- DMI-to-DRAM
- DMI-to-CPU (FSB interrupts or MSIs only)
- CPU-to-DMI
- Messaging in both directions, including Intel Vendor-specific messages
- Supports power management state change messages
- APIC and MSI interrupt messaging support
- Supports SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive and LPC bus masters

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1.2.4 I/O Controller Hub: Intel ICH7-M

The ICH7 provides extensive I/O support. Functions and capabilities include:

- PCI Express base specification, revision 1.0a support
- PCI local bus specification, revision 2.3 support for 33 MHz PCI operations (supports up to six Req/Gnt pairs)
- ACPI power management logic support
- Enhanced DMA controller, interrupt controller and timer functions
- Integrated serial ATA host controller with independent DMA operation on four ports and AHCI (ICH7R support
- USB host interface with support for eight USB ports; four UHCI host controllers; one EHCI high-speed USB 2.0 host controller
- System Management Bus (SMbus) specification, version 2.0 with additional support for I^2C devices
- Supports audio codec ’97, revision 2.3 specification (a.k.a , AC ’97 component specification, revision 2.3) which provides a link for audio and telephony codecs (up to 7 channels)
- Supports Intel high definition audio
- Supports Intel Matrix storage technology (ICH7R only)
- Supports Intel Active Management Technology

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- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

1.2.5 Azalia Audio System: ALC880

ALC880 provides 7.1 channels of outputs and multiple stereo inputs, along with flexible mixing, mute and finer gain ALC880 provides 7.1 channels of outputs and multiple stereo inputs, along with flexible mixing, mute and finer gain control functions to provide a complete integrated audio solution for PCs. Also the highest 192 KHz sample rate DACs and Realtek proprietary hardware content protection are applicable for DVD audio, which only implemented in high end consumer electronics, now is achieved by PCs with ALC880 inside. ALC880 is also the one and only high definition audio codec integrating three pairs of stereo ADCs which can support microphone array with AEC (Acoustic Echo Cancellation), BF (Beam Forming) and NS (Noise Suppression) technology simultaneously to significantly improve recording quality for conference call. With this unique feature (3 pairs of Stereo ADCs), ALC880 can perform the ultimate performance of HAD like using S/PDIF to output analog data or multiple recording application.

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Feathers:

- High performance DACs with 95 dB S/N ratio
- Meets performance requirements for audio on PC2001 systems
- 8 channels of DAC support 16/20/24-bit PCM format for 7.1 audio solution
- 3 stereo ADCs support 16/20-bit PCM format, two for microphone array, one for legacy mixer recording

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- Supports 44.1/48/96/192 KHz DAC sample rate
- All ADCs support 44.1/48/96 KHz sample rate
- Applicable for 4 ch/192 KHz and 6 ch/96 KHz DVD-Audio solution
- Up to 4 channels of microphone input are supported for AEC/BF application
- Support power off CD function
- Support external PCBEEP input and built in BEEP generator
- PCBEEP Pass-Through when link is in RESET state
- Software selectable 2.5 V/3.75 V VREFOUT
- Default 6 VREFOUTs are supported, additional 4 VREFOUTs are capable by sharing un-used analog I/O pins
- 2 jack detection pins each supports up to 4 jacks plugging can be detected
- 16/20/24-bit S/PDIF-OUT supports 44.1/48/96 KHz sample rate
- 16/20/24-bit S/PDIF-IN supports 44.1/48/96 KHz sample rate
- Optional EPAD (External Amplifier Power Down) is supported
- Power support digital 3.3 V, analog 3.3 V/5.0 V
- Power management and enhanced power saving features

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- 48-pin LQFP package is compatible with AC'97
- Reserve analog mixer architecture is backward compatible with AC'97
- –64 dB ~ +30 dB with 1dB resolution of mixer gain to achieve finer volume control
- Impedance sensing capability for each re-tasking jack support power off CD function
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built in headphone amplifier for each re-tasking jack
- Support external volume knob control
- Support 2 GPIO (General Purpose Input/Output) for customized application
- Hardware content protection for DVD-Audio supporting

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1.2.6 MDC: Azalia MDC Modem Card

Feathers:

- AC'97/MC'97 2.2 compliant
- MDC Modem support current sense, whenever the current on the line exceeds approximately 150 mA and should immediately go back on hook

- ITU-T V.92 PCM Upstream and V.90 data rates with auto0fallback to V.34, V.32ter V.32 bis and fallbacks
- Virtual com port with a through put of up to 460.8 Kbps
- V.42 bis/MNP 5 data compression
- FAX send and receive rates up to 14.4kbps, V.17, V.29, V.27ter
- Hayes AT command set
- Supports V.42 error correction and V.44, V.42bis/MNP5 data compression
- FAX capabilities: ITU-T V.17, V.29, V.27ter, V.21 Ch2 and TIA/EIA 578 Class1 FAX
- Modem support wake up on ring

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1.2.7 System Flash Memory (BIOS)

- Firmware hub for Intel® 810, 810E, 815, 815E, 815EP, 820, 840, 850 chipsets
- Flexible erase capability
  - Uniform 4 KBytes sectors
  - Uniform 16 KBytes overlay blocks for SST49LF002A
  - Uniform 64 KBytes overlay blocks for SST49LF004A
  - Top boot block protection

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  - 16 KBytes for SST49LF002A
  - 64 KBytes for SST49LF004A
  - Chip-Erase for PP mode
- Single 3.0-3.6 V read and write operations
- Superior reliability
- Firmware hub hardware interface mode
  - 5-signal communication interface supporting byte read and write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top boot block
  - Block locking register for all blocks
  - Standard SDP command set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection

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1.2.8 Memory System

- 128 MB, 256 MB, 512 MB, 1 GB (x64) 200-Pin DDR2 SDRAM SODIMMs
  - JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
  - VDD=+1.8 V±0.1 V, VDDQ=+1.8 V±0.1 V
  - JEDEC standard 1.8 V I/O (SSTL_18-compatible)
  - Differential data strobe (DQS,DQS#) option
  - Four-bit prefetch architecture
  - Differential clock input (CK, CK#)
  - Command entered on each rising CK edge
  - DQS edge-aligned with data for reads
  - DQS center-aligned with data for writes
  - Duplicate output strobe (RDQS) option for x8 configuration
  - DLL to align DQ and DQS transitions with CK
  - Four internal banks for concurrent operation
  - Data Mask (DM) for masking write data

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- Programmable CAS Latency (CL): 2, 3, 4 and 5
- Posted CAS additive latency (AL): 0, 1, 2, 3 and 4
- Write latency = read latency – $1^{t}CK$
- Programmable burst lengths : 4 or 8
- Read burst interrupt supported by another read
- Write burst interrupt supported by another write
- Adjustable data – output drive strength
- Concurrent auto precharge option is supported
- Auto Refresh (CBS) and self refresh mode
- 64 ms, 8, 192-cycle refresh
- Off-Chip Drive (OCD) impedance calibration
- On-die termination (ODT)

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1.2.9 LAN

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip fast Ethernet controller that provides 32-bit performance, PCI bus master capability and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x full duplex flow control. It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management possible. The RTL8100C (L) does not support CardBus mode as the RTL8139C does. In addition to the ACPI feature, the RTL8100C(L) also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8100C(L) is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8100C(L) is ready and waiting for the magic packet or link change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse and negative pulse. The versatility of the RTL8100C(L) LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. The RTL8100C(L) also supports analog Auto-Power-down, that is, the analog part of the RTL8100C(L) can be shut down temporarily according to user requirements or when the RTL8100C(L) is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the isolate B pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and the power consumption of the RTL8100C(L) will be negligible. The RTL8100C(L) also supports an auxiliary power auto-detect function and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

- 128-pin QFP/LQFP
- Integrated fast Ethernet MAC, physical chip and transceiver in one chip
- 10 Mb/s and 100 Mb/s operation

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- Supports 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
- PCI local bus single-chip fast Ethernet controller
  - Compliant to PCI revision 2.2
  - Supports PCI clock 16.75 MHz-40 MHz
  - Supports PCI target fast back-to-back transaction
  - Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8100C(L)'s operational registers
  - Supports PCI VPD (Vital Product Data)
  - Supports ACPI, PCI power management
- Supports 25 MHz crystal or 25 MHz OSC as the internal clock source. The frequency deviation of either crystal or OSC must be within 50 PPM
- Compliant to PC99/PC2001 standard
- Supports Wake-On-LAN function and remote wake-up (Magic Packet*, LinkChg and Microsoft® wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI

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configuration space

- Includes a programmable, PCI burst size and early Tx/Rx threshold
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large (2 KBytes) independent receive and transmit FIFOs
- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) to store resource configuration, ID parameter and VPD data
- Supports LED pins for various network activity indications
- Supports loopback capability, Half/Full duplex capability
- Supports full duplex flow control (IEEE 802.3x)

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1.2.10 Keyboard System: Winbond W83L951DG

The Winbond mobile keyboard and embedded controller W83L951D/F architecture consists of a Turbo-8051 core logic controller and surrounded by various components, 2 K+256 bytes of RAM, 64 K on-chip flash, LPC host interface, 13 general purpose I/O port with 24 external interrupt source, 4 timers, 1 serial port, 2 SMBus interface for master mode, 3 PS/2 port, two 8-bit and two 16-bit PWM channels, 2 D-A and 8 A-D converters, 1 Consumer Infrared communications receiver, 2 fan tachometer, 1 real time clock generator and matrix interface. The part number with an affix of “G” is the Lead-free package product.

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- 128-pin QFP/LQFP
  - 8-bit Turbo 8052 Microprocessor code based, speed up to 24 MHz
  - 256 bytes internal RAM
  - 64 K bytes embedded programmable flash memory
  - 2 K bytes external SRAM
- Host interface
  - Software optional with LPC interface
  - Primary programmable I/O address communication port in LPC mode
  - Support SERIRQ in LPC interface
  - Support hardware fast Gate A20 and KBRST
  - Support port 92 h
- SMBus
  - Support 2 SMBus interface support master mode
- Timers

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- Support four timer signal with three pre-scalars
- Timer 1 and 2 Shard the Same Pre-scalar and are Free-Running Only
- Timer X and Y Have Individual Pre-scalar and Support up to Four Control Modes, Free Running, Pulse Output, Event Counter and Pulse Width Measurement

➢ PWM

- Support four PWM Channels
- PWM 0 and 1 are 8-bit and programmable frequency from 62 Hz to 7.5 KHz
- PWM 2 and 3 are 16-bit and programmable frequency from 6 Hz to 3 MHz

➢ Fan Tachometer

- Support two fan tachometer inputs

➢ A/D Converter

- Firmware programmable optional with 10-bit or 8-bit resolution, support eight channels

➢ D/A Converter

- 8-bit Resolution, support two channels

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- PS2
  - Support three hardware PS2 channels
  - Optional PS2 clock inhibit by hardware or firmware
- Keyboard Controller
  - Support 16*8 keyboard Matrix-scan, expanding to 18*8 and 20*8
- GPIO
  - Support 104 useful GPIO pins totally and Bit–addressable to facility firmware coding
- Flash
  - Support external On-Board 64 K flash via matrix interface (GP0, 1, 3)
- CIR
  - Support decoding for the NEC consumer IR remote control format
- RTC
  - Real time clock generator with 32.768 KHz input
- ACPI

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- Support ACPI appliance secondary programmable I/O address communication port in LPC mode

➢ Package

- 128-pin QFP and 128-pin LQFP package options

1.2.11 Hard Disk Drive

8258I can support SATA HDD by equipped different HDD transition board.

SATA HDD: The SATA function in the ICH7 has dual modes of operation to support different operating system conditions. In the case of native IDE enabled operating systems, the ICH7 has separate PCI functions for serial and parallel ATA (enhanced mode). To support legacy operating systems, there is only one PCI function for both the serial and parallel ATA ports if functionality from both SATA and PATA devices is desired (combined mode). SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.

- Up-to 150 MB/sec bus speed (Serial ATA generation 1)
- Compliant with Serial ATA 1.0a specification and Serial ATA 2 extensions 1.0
- Supports 48-bit LBA addressing
- Supports native DMA queued command (first party DMA queued)

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- Supports legacy DMA queued command
- Supports staggered spin-up function
- Supports Hot-Plug features
- Supports Serial ATA power management (host initiated partial/slumber)

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1.3 Other Functions

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Wireless LAN ON/OFF	Wireless LAN ON/OFF
Fn + F2	Bluetooth ON/OFF	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F10	Mute	Audio Mute
Fn + F11	Display Off/On	Toggle Display on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

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1.3.2 Power on/off/suspend/resume button

- APM Mode
  - At APM mode, power button is on/off system power
- ACPI Mode

- At ACPI mode, windows power management control panel set power button behavior. You could set “standby”, “power off” or “hibernate” (must enable hibernate function in power management) to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring cover switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

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1.3.4 LED Indicators

- Six LED indicators

From left to right that indicates Power, Battery Status, HDD/ODD, NUM LOCK, CAP LOCK, WLAN.

Power: This LED lights blue when the notebook was powered by AC or battery power line, flashes (on 1 second,

off 1 second) when entered suspend to RAM state. The LED is off when the notebook is in power off state.

Battery status: With battery operation, this LED stays off. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 seconds. When AC is connected, this indicator stays off if the battery pack is fully charged or red if the battery is being charged.

System has four status LED indicators at front side which to display system activity: HDD/ODD, NUM LOCK, CAPS LOCK and WLAN.

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1.3.5 Battery Status

1.3.5.1 Battery Warning

- System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low
- Battery Warning: Capacity below 10%, Battery Status LED flashes per second, system beeps per 2 seconds
- System will suspend to HDD after 2 Minutes to protect users data

1.3.5.2 Battery Low State

After battery warning state, and battery capacity is below 5%, system will generate beep sound for twice per second.

1.3.5.3 Battery Dead State

When the battery voltage level reaches 8.56 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan power on/off management

Fan is controlled by W83L951DG embedded controller-using ADM1032 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster fan speed.

1.3.7 CMOS Battery

CR2032 3 V 220 mAh lithium battery, when AC in or system main battery inside, CMOS battery will consume no power.
AC or main battery not exists, CMOS battery life at less (220 mAh/5.8 uA) 4 years

1.3.8 I/O Ports

- One Power Supply Jack
- One External CRT Connector For CRT Display
- Supports four USB port for all USB devices

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- One modem RJ-11 phone jack for PSTN line
- One RJ-45 for LAN
- One SPDIF jack
- One Microphone input jack
- One S-Video (PAL/NTSC) connector
- One Express card jack
- One Mini PCI-E jack for WLAN card

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1.3.9 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Power Management

The 8258I system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported

1.4.1 System Management Mode

- Full on mode

  In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

- Doze mode

  In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability. The CPU power consumption and temperature is lower in this mode.

- Standby mode

  For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

  - CPU: Stop grant
  - LCD: Backlight off

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- HDD: Spin down

➢ Suspend to DRAM/HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- Suspend to DRAM
  - CPU: Off
  - Intel 945GM: Partial off
  - VGA: Suspend
  - Audio: Off
  - SDRAM: Self refresh
- Suspend to HDD
  - All devices are stopped clock and power-down
  - System status is saved in HDD
  - All system status will be restored when powered on again

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1.4.2 Other Power Management Functions

- HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

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1.5 Appendix 1: Intel ICH7-M GPIO Definitions-1

Pin name	Current Define	Default Input/output	Function	Power Well
GPIO0	PM_BMBUSY#	I	Bus Master busy	CORE
GPIO1	PCI_REQ5#	I	X	CORE
GPIO2	PCI_INTE#	I	PCI interrupt for LAN	CORE
GPIO3	PCI_INTF#	I	X	CORE
GPIO4	PCI_INTG#	I	X	CORE
GPIO5	PCI_INTH#	I	X	CORE
GPIO6	SMB_SEL	I	ECO Function	CORE
GPIO7	SCI#	I	System Control Interrupt	CORE
GPIO8	EXTSMI#	I	SMI signal for chipset	RESUME
GPIO9	X	I	X	RESUME
GPIO10	X	I	X	RESUME
GPIO11	SMBALERT#	Native	SMBus alert	RESUME
GPIO12	X	I	X	RESUME
GPIO13	X	I	X	RESUME
GPIO14	X	I	X	RESUME
GPIO15	X	I	X	RESUME
GPIO16	DPRSLPVR	O	Lower power in deeper sleep	CORE
GPIO17	X	O	X	CORE
GPIO18	STOP_PCI#	O	PCI stop	CORE

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1.5 Appendix 1: Intel ICH7-M GPIO Definitions-2

Continue to the previous page

Pin name	Current Define	Default Input/output	Function	Power Well
GPIO19	PANEL_ID1	I	X	CORE
GPIO20	STOP_CPU#	O	CPU stop	CORE
GPIO21	PANEL_ID0	I	X	CORE
GPIO22	PCI_REQ4#	Native	X	CORE
GPIO23	X	Native	X	CORE
GPIO24	X	O	X	RESUME
GPIO25	X	O	X	RESUME
GPIO26	PWM_PWR_ON	O	ECO Switch	RESUME
GPIO27	SPK_OFF	O	Speaker turns off	RESUME
GPIO28	X	O	X	RESUME
GPIO29	X	Native	X	RESUME
GPIO30	X	Native	X	RESUME
GPIO31	X	Native	X	RESUME
GPIO32	PCLKRUN#	O	Clock run	CORE
GPIO33	WIRELESS_PD#	O	X	CORE
GPIO34	X	O	X	CORE
GPIO35	X	O	X	CORE
GPIO36	PANEL_ID2	I	X	CORE
GPIO37	X	I	X	CORE
GPIO38	MB_ID0	I	Mother Board ID	CORE
GPIO39	MB_ID1	I	Mother Board ID	CORE
GPIO48	X	Native	X	CORE
GPIO49	HPWRGD	Native	CPU power good	V_CPU_IO

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1.6 Appendix W83L951DG KBC GPIO Pins Definitions-1

Pin Name	Pin	951 Pin Definitions	I/O	Function	8258I
RESET#	50	RESET#	I	951 Chip Reset	
TEST#	124	TEST#	I	Normal operation by direct external rom	
XIN	122	System Clock	I	Crystal use 24 MHZ	
XOUT	123	System Clock	I	Crystal use 24 MHZ	
XCIN	125	RTC Clock	I	Crystal use 32.768 KHZ	
XCOUT	126	RTC Clock	I	Crystal use 32.768 KHZ	
VCC1	23		I	+3.3 V	
GND	32		I	Ground	
VCC2	60		I	Please connect it to +3.3 V from LPC interface	
VCC1	49		I	+3.3 V	
GND	55		I	Ground	
VCC1	78		I	+3.3 V	
GND	69		I	Ground	
AVCC	112		I	Analog Power	
AVref	103		I	Analog reference voltage	
AGND	115		I	Analog Ground	
LPC Interface					
LAD3	59	LPC_AD3	I/O	LPC Address/Data I/O 3	
LAD2	58	LPC_AD2	I/O	LPC Address/Data I/O 2	
LAD1	57	LPC_AD1	I/O	LPC Address/Data I/O 1	
LAD0	56	LPC_AD0	I/O	LPC Address/Data I/O 0	
SERIRQ	54	SERIRQ		Serial Host Interrupt	
LRESET#	53	LPC_RESET#		LPC Reset	
LFRAME#	52	LPC_FRAME#		LPC Frame	
LCKL	51	PCICLK		LPC Clock	
Port 0					
GP00	94	KB OUT 0	O	Key matrix scan output 0	
GP01	93	KB OUT 1	O	Key matrix scan output 1	

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1.6 Appendix W83L951DG KBC GPIO Pins Definitions-2

Continue to the previous page

Pin Name	Pin	951 Pin Definitions	I/O	Function	8258I
GP02	92	KB OUT 2	O	Key matrix scan output 2	
GP03	91	KB OUT 3	O	Key matrix scan output 3	
GP04	90	KB OUT 4	O	Key matrix scan output 4	
GP05	89	KB OUT 5	O	Key matrix scan output 5	
GP06	88	KB OUT 6	O	Key matrix scan output 6	
GP07	87	KB OUT 7	O	Key matrix scan output 7	
Port 1					
GP10	86	KB OUT 8	O	Key matrix scan output 8	
GP11	85	KB OUT 9	O	Key matrix scan output 9	
GP12	84	KB OUT 10	O	Key matrix scan output 10	
GP13	83	KB OUT 11	O	Key matrix scan output 11	
GP14	82	KB OUT 12	O	Key matrix scan output 12	
GP15	81	KB OUT 13	O	Key matrix scan output 13	
GP16	80	KB OUT 14	O	Key matrix scan output 14	
GP17	79	KB OUT 15	O	Key matrix scan output 15	
Port 2					
GP20	77	Key Type0	I	Keyboard Languag select	KBD_US/JP#
GP21	76	Key Type1	I	Keyboard Languag select	PWRGD
GP22	75	M/B ID0	I	Reserve for M/B version	CRT_DT#
GP23	74	M/B ID1	I	Reserve for M/B version	BATTERY_TYPE
GP24/PWM0	73				+3/5V_GD
GP25/PWM1	72				KBC_BEEP
GP26/PWM2	71	FAN0_ON#	O	Fan0 power PWM control	FANON
GP27/PWM3	70	FAN1_ON#	O	Fan1 power PWM control	
Port 3					
GP30	102	KEY IN 0	I	Key matrix input 0	
GP31	101	KEY IN 1	I	Key matrix input 1	

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1.6 Appendix W83L951DG KBC GPIO Pins Definitions-3

Continue to the previous page

Pin Name	Pin	951 Pin Definitions	I/O	Function	8258I
GP32	100	KEY IN 2	I	Key matrix input 2	
GP33	99	KEY IN 3	I	Key matrix input 3	
GP34	98	KEY IN 4	I	Key matrix input 4	
GP35	97	KEY IN 5	I	Key matrix input 5	
GP36	96	KEY IN 6	I	Key matrix input 6	
GP37	95	KEY IN 7	I	Key matrix input 7	
Port 4					
GP40/FAN_TACH0	68	Fan0_SPD	I	Fan0 speed input	FAN_SPEED
GP41/FAN_TACH1	67	Fan1_SPD	I	Fan1 speed input	
GP42/RXD	66	RXD	I	For Firmware debug	KBC_RX
GP43/TXD	65	TXD	O	For Firmware debug	KBC_TX
GP44/KBRST#	64	KBC_HRCIN#	O	CPU Reset	HRCIN#
GP45/GATE_A20	63	A20_GATE	O	System A20 Gate	A20GATE
GP46/CLKRUN#	62	PM_CLKRUN#		LPC Clock Run	PCLKRUN#
GP47/LPCPD#	61	PM_SUS_START		LPC Power-Down	LPCPD
Port 5					
GP50	121	LSMI#	O	External SMI#	EXTSMI
GP51	120	LSCI	O	Need invert to SCI# sending to SouthBridge	H8_SCI
GP52	119	KBC_WAKE#	O	Wake-up SouthBridge at ACPI mode	H8_WAKE_UP#
GP53	118	KBC_THRM#	O	Thermal throttling control to SouthBridge	H8_THRM#
GP54	117				WIRE_EN
GP55	116				BLT_DT
GP56/DA0	114	BLADJ	O	Backlight inverter brightness adjust	BLADJ
GP51/DA1	113	I-CTRL	O	Charging current adjust	I_CTRL
Port 6					
GP60/AD0	111	BATT_VOLT	I	Battery voltage meansure	BAT_VOLT
GP61/AD1	110	I-Limit	I	I-Limit function	I_LIMIT

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1.6 Appendix W83L951DG KBC GPIO Pins Definitions-4

Continue to the previous page

Pin Name	Pin	951 Pin Definitions	I/O	Function	8258I
GP62/AD2	109	3V/PWROK	I	Monitor system on/off state	
GP63/AD3	108	Vtt	I	System Vtt voltage	KBC_VCCP
GP64/AD4	107	BATT_TEMP	I	Battery thermister temperature	BAT_TEMP
GP65/AD5	106	V_Core	I	CPU Vcore voltage	KBC_CPUCORE
GP66/AD6	105	I_Charge	I	Reserve for Internal Gauge	
GP67/AD7	104	I_Discharge	I	Reserve for Internal Gauge	
Port 7					
GP70/PS2_1CLK	48	T_CLK	I/O	TouchPAD Clock	T_CLK
GP71/PS2_1DAT	47	T_DATA	I/O	TouchPAD Data	T_DATA
GP72/PS2_2CLK	46	T_CLK2		Option for second PS2 interface	BLT_EN#
GP73/PS2_2DAT	45	T_DATA2		Option for second PS2 interface	POWEROK
GP74/PS2_3CLK	44				ECOBTN_SW#
GP75/PS2_3DAT	43				PWM_PWR
GP76/SDA0	42	BATT_DATA	I/O	SMBus Data	BAT_DATA
GP77/SCL0	41	BATT_CLK	I/O	SMBus Clock	BAT_CLK
Port 8					
GP80/SDA1	40	SMB_DATA1		Reserve for SMBus Data 1	H8_THRM_DATA
GP81/SCL1	39	SMB_CLK1		Reserve for SMBus Clock 1	H8_THRM_CLK
GP82/CNTR0	38			Reserve for Fan0 Speed detect	FAN_SPEED_C
GP83/CNTR1	37	Prochot#	O	Indicate Intel CPU to do throttle function	
GP84/CIR_RX	36			CIR Receiver	
GP85	35	LEARNING#	O	Auto-Learning	LEARNING
GP86	34	CHARGING	O	Battery charge control	CHARGING
GP87	33	KBC_ENABKL	O	Enable Backlight	H8_ENABKL
Port9					
GP90	31	KBC_PWRON_VDD3S	O	Turn on VDD3.3 and VDD1.5	KBC_PWRON_VDD3S
GP91	30	KBC_RSMRST	O	SouthBridge RSMRST#	

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1.6 Appendix W83L951DG KBC GPIO Pins Definitions-5

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Pin Name	Pin	951 Pin Definitions	I/O	Function	8258I
GP92	29	SB_PWRBTN#	O	SouthBridge power button	
GP93	28	PWRON_1.35V_1.5V	O	System power on	SUSB1.5V
GP94	27	SW_VDD3	O	VDD3 power source switch	SUSC1.8V
GP95	26	PWROK	O	Reserve for other power sequence pin	SW_VDD3
GP96	25	PWRON_VCORE	O	Reserve for other power sequence pin	SUSB_VCC_CORE
GP97	24	PWRON_1.8V_1.25V	O	Reserve for other power sequence pin	SUSB0.9V
Port A					
GPA0/EXTINT10	22	PWRON_5V	O	Reserve for other power sequence pin	OCO5V
GPA1/EXTINT11	21	PWRON_3V	O	Reserve for other power sequence pin	OCO3V
GPA2/EXTINT12	20	PWRON_2.5V	O	Reserve for other power sequence pin	SUSB2.5V
GPA3/EXTINT13	19	PWRON_1.05V	O	Reserve for other power sequence pin	SUSB_VCCP
GPA4/EXTINT14	18	PWRON_+3V_+5V	O	Reserve for other power sequence pin	SUSB3V
GPA5/EXTINT15	17			Reserve for other power sequence pin	SUSB5V
GPA6/EXTINT16	16			Reserve for other power sequence pin	ICH_PWRBTN#
GPA7/EXTINT17	15			Reserve for other power sequence pin	KBC_RSMRST
Port B					
GPB0/EXTINT20	14	LED_CAP#	O	Capitals Lock LED indicator	CAP#
GPB1/EXTINT21	13	LED_NUM#	O	Numeral Lock LED indicator	NUM#
GPB2/EXTINT22	12	LED_SCR#	O	Scroll Lock LED indicator	SCROLL#
GPB3/EXTINT23	11	LED_BATT_R#	O	Battery Charger Red LED indicator	BATT_R#
GPB4/EXTINT24	10	LED_BATT_G#	O	Battery Charger Green LED indicator	BATT_G#
GPB5/EXTINT25	9	LED_AC_PWR#	O	AC Power LED indicator	AC_LED#
GPB6/EXTINT26	8	LED_BATT_PWR#	O	Battery Power LED indicator	AC_BAT_POWER#
GPB7/EXTINT27	7			Reserve for other LED indicator	ECOBTN_LED#
Port C					
GPC0/EXTINT30	6	PWRBTN#	I	Power Button	PWRBTN

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1.6 Appendix W83L951DG KBC GPIO Pins Definitions-6

Continue to the previous page

Pin Name	Pin	951 Pin Definitions	I/O	Function	8258I
GPC1/EXTINT31	5	KBC_SUSB	I	Invert from SUSA# to wake up KBC when system resumed by MDC modem and internal LAN. Inform system power management status.	KBC_SUSB#
GPC2/EXTINT32	4	KBC_SUSC#	I	System to S4 (soft off) or S5	SUSC#
GPC3/EXTINT33	3	KBC_ADEN#	I	AC adaptor in detect	ADEN#
GPC4/EXTINT34	2	BATT_DEAD#	I	Battery low detect	BATT_DEAD#
GPC5/EXTINT35	1	COVER_SW#	I	Cover switch	LIDSW#
GPC6/EXTINT36	128			Reserve for other Interrupt pin	
GPC7/EXTINT37	127			Reserve for other Interrupt pin	

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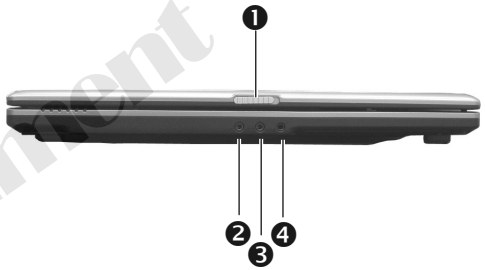
2. System View and Disassembly

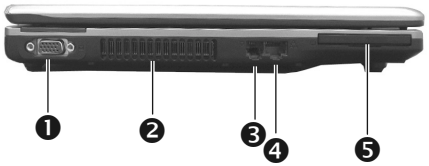
2.1 System View

2.1.1 Front View



❶ Top Cover Latch
❷ External MIC In Connector
❸ Line In Connector
❹ Line Out/SPDIF Connector

2.1.2 Left-side View



❶ CRT Connector
❷ Ventilation Openings
❸ RJ11 Connector
❹ RJ45 Connector
❺ Express Card Socket

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2.1.3 Right-side View

❶ ODD
❷ USB Ports*2

2.1.4 Rear View

❶ Power Connector
❷ S-Video Port
❸ USB Ports*2
❹ Kensington Lock

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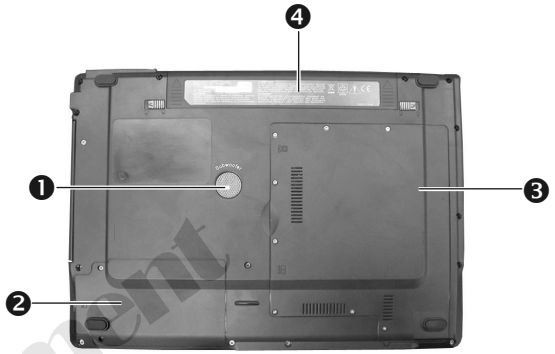
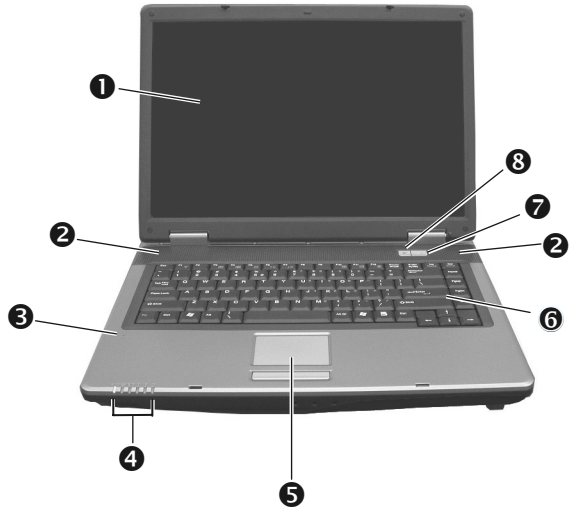
2.1.5 Bottom View

❶ Subwoofer Speaker
❷ Hard Disk Drive
❸ CPU & DDR2 SO-DIMM & Modem
❹ Battery Park



2.1.6 Top-open View

❶ LCD Screen
❷ Stereo Speaker Set
❸ Internal MIC
❹ Device LED Indicators
❺ Touch Pad
❻ Keyboard
❼ Power Button
❽ ECO Button



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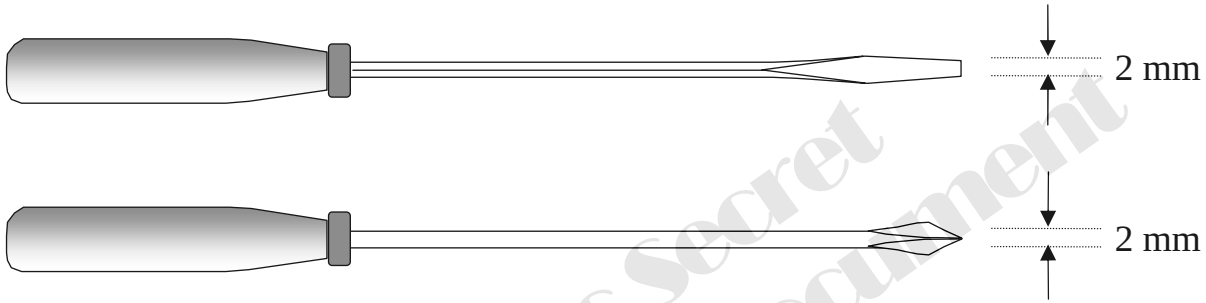
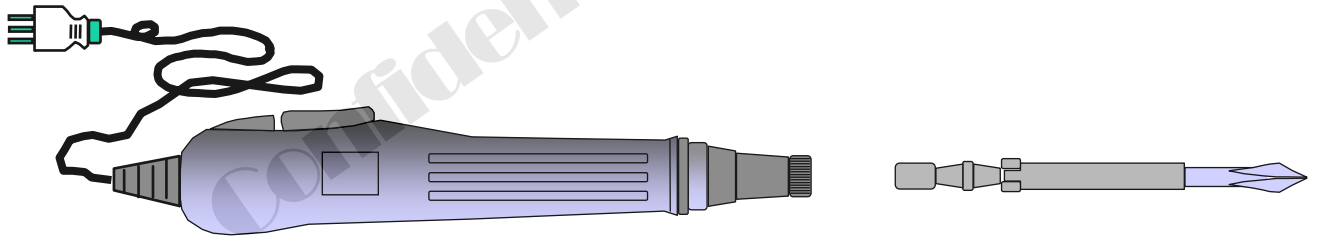
2.2 Tools Introduction

1. Minus screw driver for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm^2	#0

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2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

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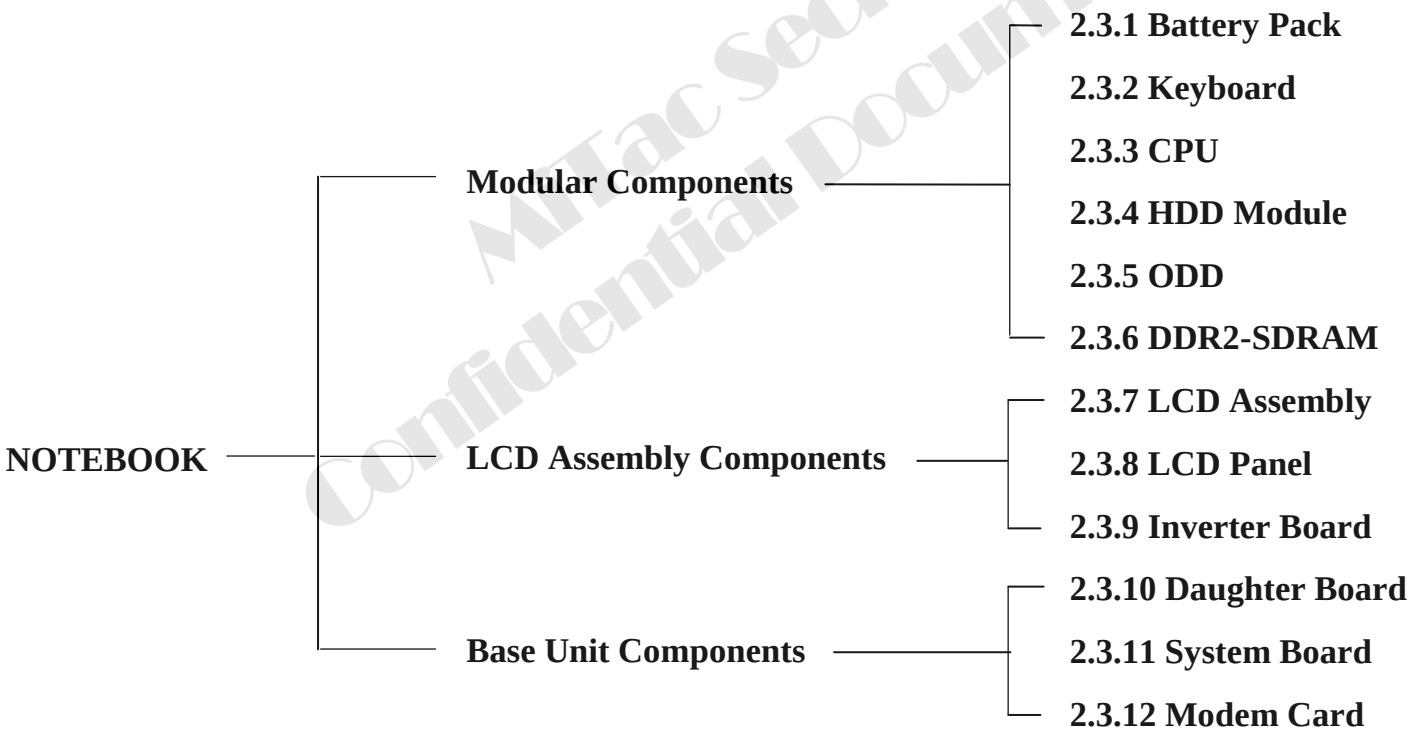

2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide two release lever outwards to the “unlock” ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

Figure 2-1 Remove the battery pack

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Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” ( ) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Push firmly to slide the easy start buttons cover to the right (❶). Then lift the easy start buttons cover up (❷). (Figure 2-2)
3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-3)

Figure 2-2 Remove the keyboard cover

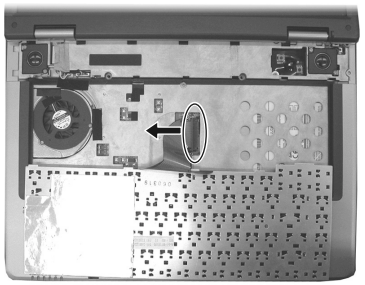

Figure 2-3 Remove the keyboard

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Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the easy start buttons cover.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove eight screws fastening the CPU cover. (Figure 2-4)
3. Remove four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-5)

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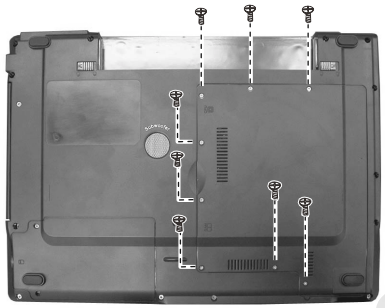

Figure 2-4 Remove eight screws

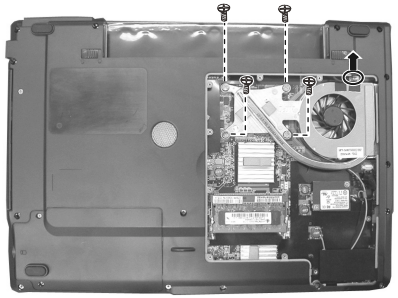

Figure 2-5 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-6)

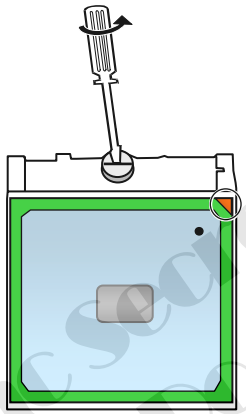

Figure 2-6 Remove the CPU

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Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with seven spring screws.
3. Replace the CPU cover and secure with eight screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove two screws fastening the HDD compartment cover. (Figure 2-7)
3. Remove one screw fastening the HDD module. Slide the HDD module out of the compartment. (Figure 2-8)

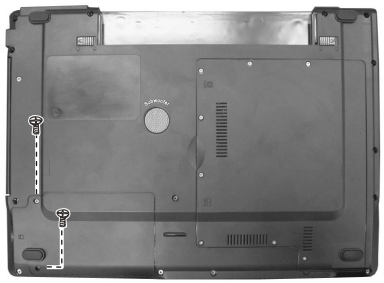

Figure 2-7 Remove the HDD compartment cover

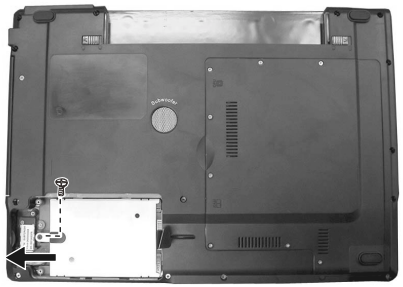

Figure 2-8 Remove HDD module

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4. Remove four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-9)

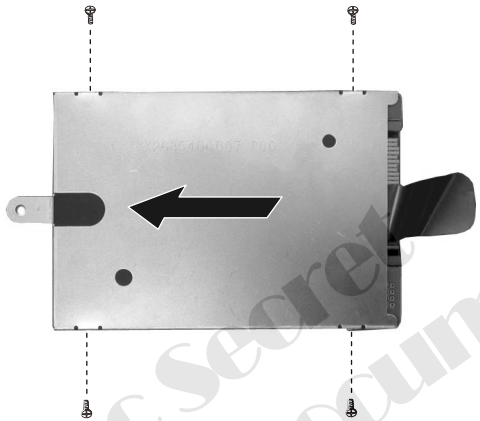

Figure 2-9 Remove hard disk drive

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Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 ODD

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove one screw fastening the ODD. (Figure 2-10)
3. Insert a small rod, such as a straightened paper clip, into ODD's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the ODD by holding the tray that pops out (❷). (Figure 2-10)

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Figure 2-10 Remove the ODD

Reassembly

1. Push the ODD into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.6 DDR2-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove eight screws fastening the CPU cover. (Refer to step 2 of section 2.3.3 Disassembly)

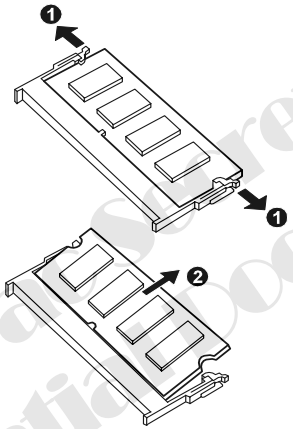

Figure 2-11 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-11)

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Reassembly

1. To install the DDR2, match the DDR2's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR2 into position.
2. Replace the CPU cover and secure with eight screws. (Refer to step 3 of section 2.3.3 Reassembly)
3. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.7 LCD Assembly

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.3.1 and 2.3.2 Disassembly)
2. Remove eight screws fastening the CPU cover. (Refer to step 2 of section 2.3.3 Disassembly)
3. Separate the antenna from the system board. (Figure 2-12)
4. Remove two hinge covers, disconnect two cables from the system board then carefully pull the antenna wires out. (Figure 2-13)

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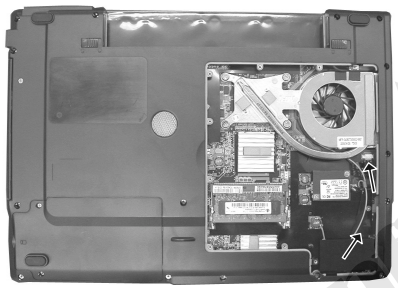

Figure 2-12 Separate the antenna

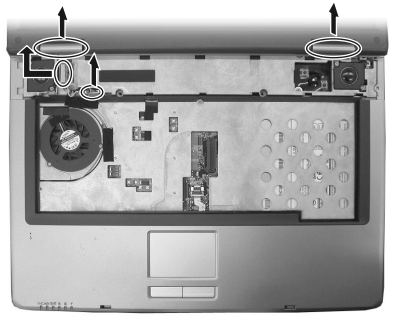

Figure 2-13 Remove two hinge covers and disconnect two cables

5. Remove four screws, then free the LCD assembly. (Figure 2-14)

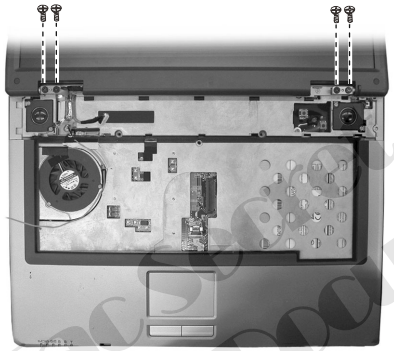

Figure 2-14 Free the LCD assembly

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Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna wires back.
3. Reconnect two cables to the system board. Then replace two hinge covers.
4. Replace the keyboard and battery pack. (Refer to sections 2.3.2 and 2.3.1 Reassembly)

2.3.8 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.7 Disassembly)
2. Remove two screws on the corners of the panel. (Figure 2-15)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove six screws and disconnect the cable. (Figure 2-16)

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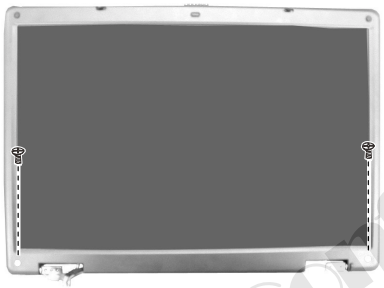

Figure 2-15 Remove LCD cover

Figure 2-16 Remove six screws and disconnect the cable

5. Remove eight screws that secure the LCD brackets. (Figure 2-17)
6. Disconnect the cable to free the LCD panel. (Figure 2-18)

Figure 2-17 Remove eight screws

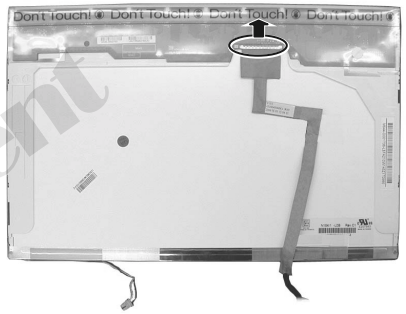

Figure 2-18 Free the LCD panel

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Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with eight screws.
3. Replace the LCD panel into LCD housing and secure with six screws.
4. Reconnect one cable to inverter board.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, keyboard and battery pack. (See sections 2.3.7, 2.3.2 and 2.3.1 Reassembly)

2.3.9 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.7 Disassembly)
2. Remove the LCD cover and LCD panel. (Refer to the steps 1-4 of section 2.3.8 Disassembly)
3. Remove three screws fastening the inverter board to free it. (Figure 2-19)

Figure 2-19 Free the inverter board

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Reassembly

1. Fit the inverter board back into place and secure with three screws.
2. Replace the LCD panel and LCD cover. (Refer to section 2.3.8 Reassembly)
3. Replace the LCD assembly. (Refer to section 2.3.7 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.3.2 and 2.3.1 Reassembly)

2.3.10 Daughter Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, ODD, DDR2 and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.7 Disassembly)
2. Remove fifteen screws. (Figure 2-20)
3. Disconnect two speakers' cables and touch pad cable from the system board and remove four screws. (Figure 2-21)

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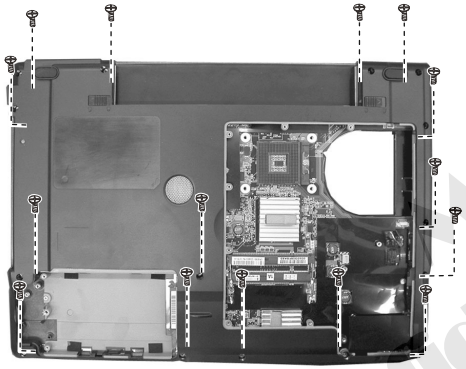

Figure 2-20 Remove fifteen Screws

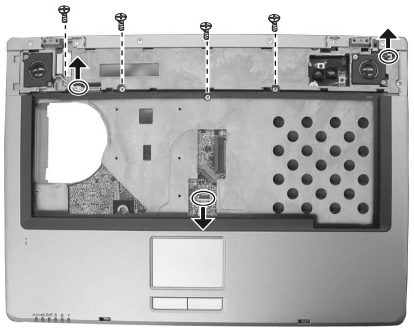

Figure 2-21 Disconnect two cables and remove four screws

4. Remove two screws fixing the system board. Then free the cover assembly. (Figure 2-22)
5. Remove one screw fixing the daughter board. (Figure 2-23)

Figure 2-22 Remove two hex nuts

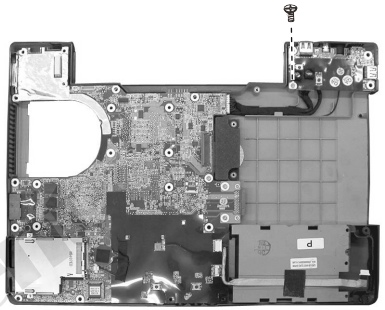

Figure 2-23 Free the system board

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6. Disconnect two daughter board cables. Then free the daughter board. (Figure 2-24)

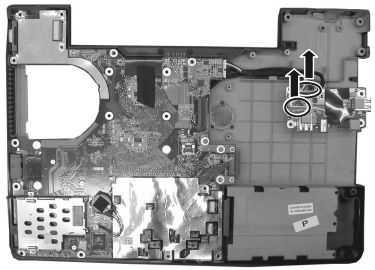

Figure 2-24 Disconnect two cables

Reassembly

1. Replace the daughter board and reconnect two cables.
2. Secure with one screw.
3. Replace the cover assembly and secure with four screws. Reconnect two speakers' cables and touch pad cable.
4. Turn over the base unit. Secure with fifteen screws and reconnect two hex nuts.
5. Replace the LCD assembly, DDR2, ODD, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

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2.3.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, ODD, DDR2 and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6 and 2.3.7 Disassembly)
2. Remove three screws, then free the mother board. (Figure 2-25)

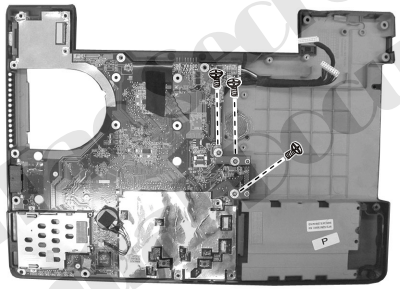

Figure 2-25 Remove three screws

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Reassembly

1. Replace the system board and reconnect three screws.
2. Replace the cover assembly and secure with four screws to fix the system board. Reconnect two speakers' cables and touch pad cable.
3. Turn over the base unit. Secure with fifteen screws and reconnect two hex nuts.
5. Replace the LCD assembly, DDR2, ODD, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.12 Modem Card

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, ODD, DDR2, LCD assembly and system board. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.11 Disassembly)
2. Disconnect the cable and remove two screws, then free the modem card. (Figure 2-26)

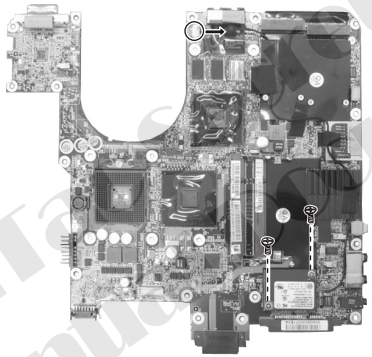

Figure 2-26 Remove the modem card

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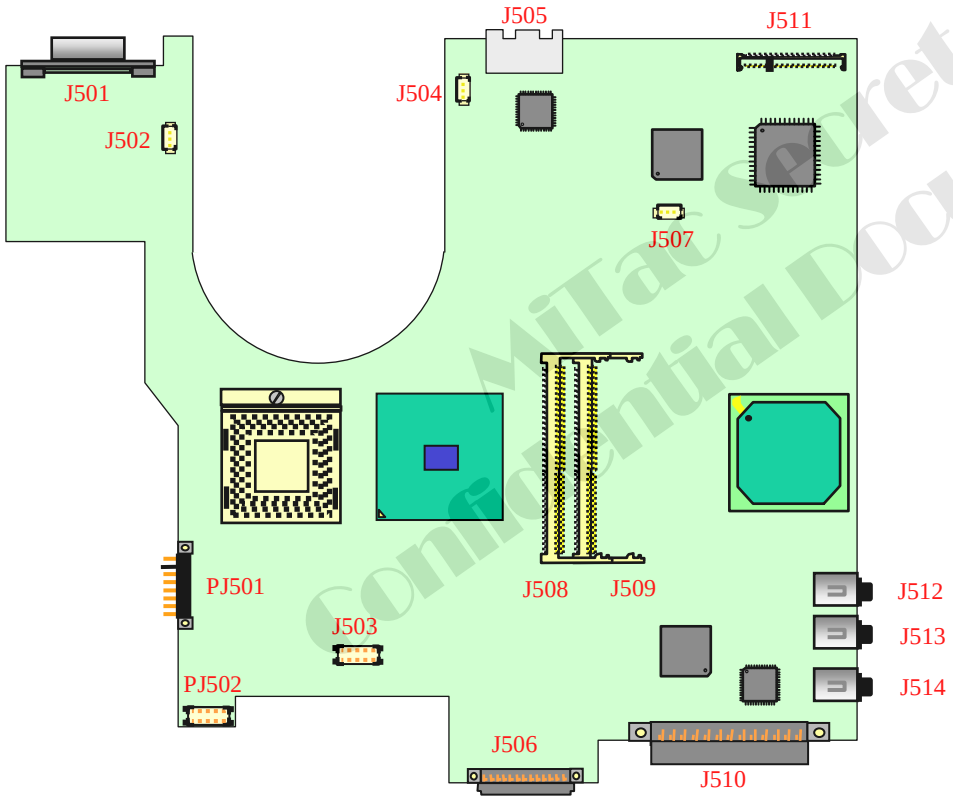
Reassembly

1. Replace the modem card back into the system board and secure with two screws, then reconnect the cable.
2. Replace the system board, LCD assembly, DDR2, ODD, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

3. Definition & Location of Connectors/Switches

3.1 Mother Board (Side A)



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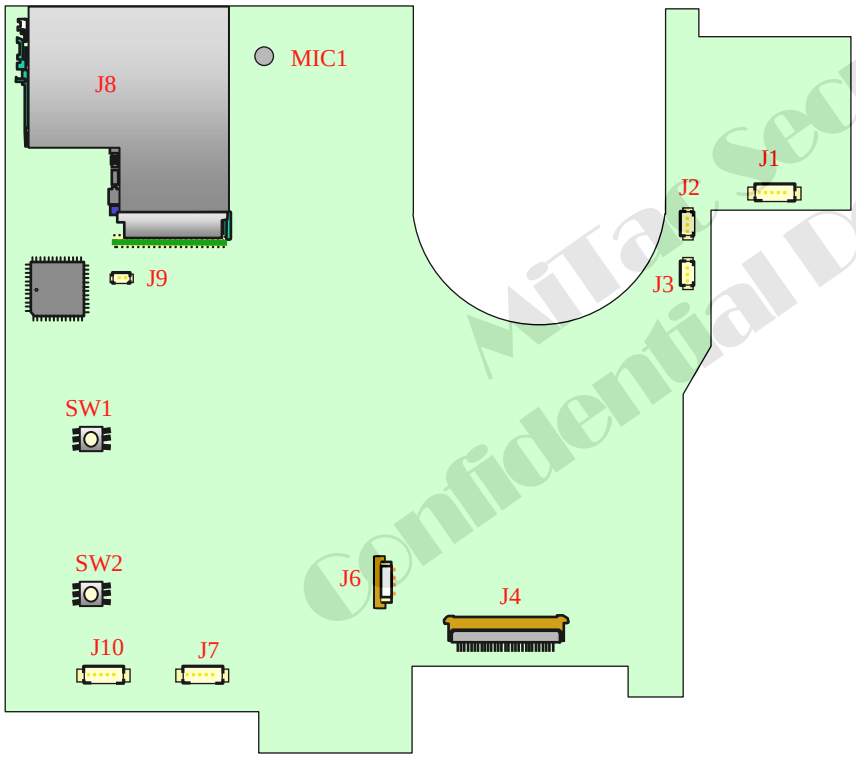
- **J501: CRT Connector**
- **PJ501: Battery Connector**
- **J502: Fan Connector**
- **PJ502, J503: MB to DB Connector**
- **J504: MDC Jump Wire Connector**
- **J505: RJ11/RJ45 Connector**
- **J506: ODD Connector**
- **J507: MDC Connector**
- **J508, J509: DDR2 SO-DIMM Socket**
- **J510: HDD Connector**
- **J511: Mini PCI-E Connector**
- **J512: External MIC In Connector**
- **J513: Line In Connector**
- **J514: Line Out Connector**

3. Definition & Location of Connectors/Switches

3.1 Mother Board (Side B)



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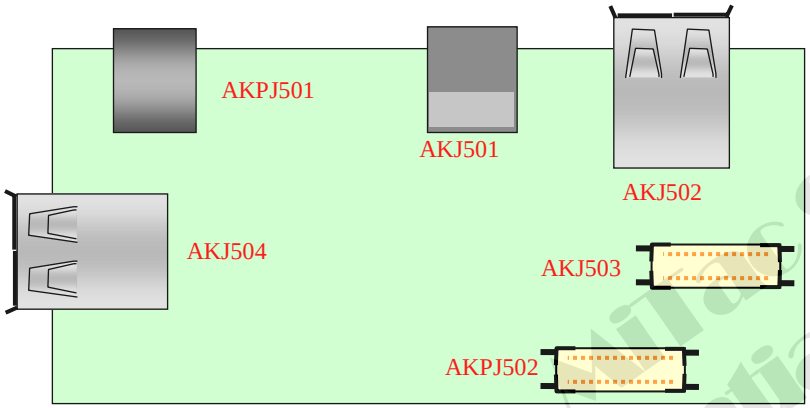
- J1: LCD Connector
- J2: Left Audio Channel Connector
- J3: LCD Inverter Board Connector
- J4: Internal Keyboard Connector
- J6: Touch Pad Connector
- J7: Blue Tooth Connector
- J8: Express Card Socket
- J9: CMOS Battery Connector
- J10: X10 Connector

- SW1: Touch Pad Left Button
- SW2: Touch Pad Right Button

3. Definition & Location of Connectors/Switches

3.2 Daughter Board (Side A)



- **AKPJ501: Power Jack**
- **AKPJ502, AKJ503: DB to MB Connector**
- **AKJ501: S-Video Port**
- **AKJ502, AKJ504: USB Port**

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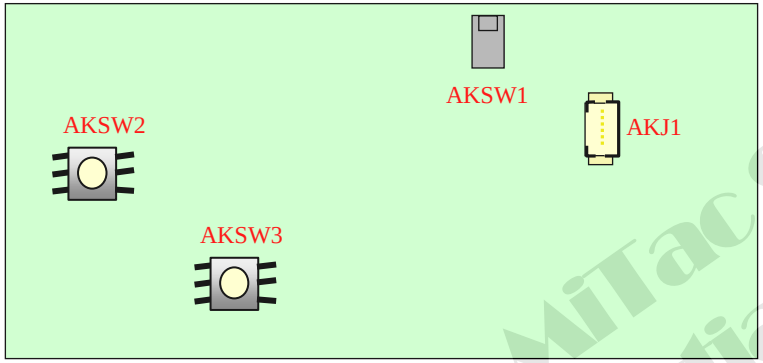
3. Definition & Location of Connectors/Switches

3.2 Daughter Board (Side B)



- **AKJ1: Right Audio Channel Connector**
- **AKSW1: LID Switch**
- **AKSW2: ECO Button**
- **AKSW3: Power Switch Button**

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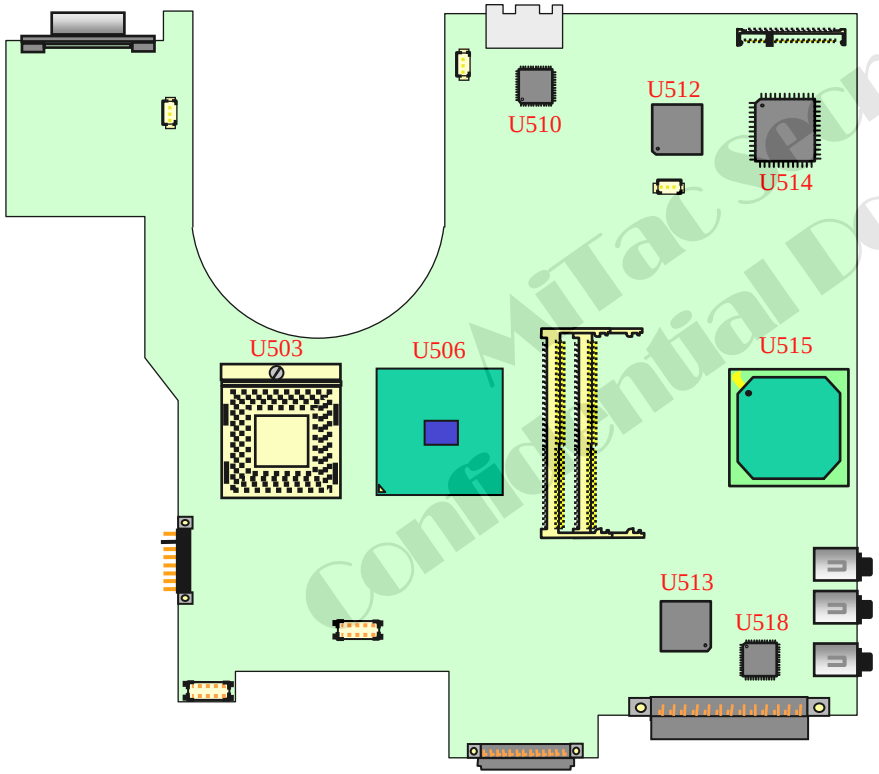
4. Definition & Location of Major Components

4.1 Mother Board (Side A)



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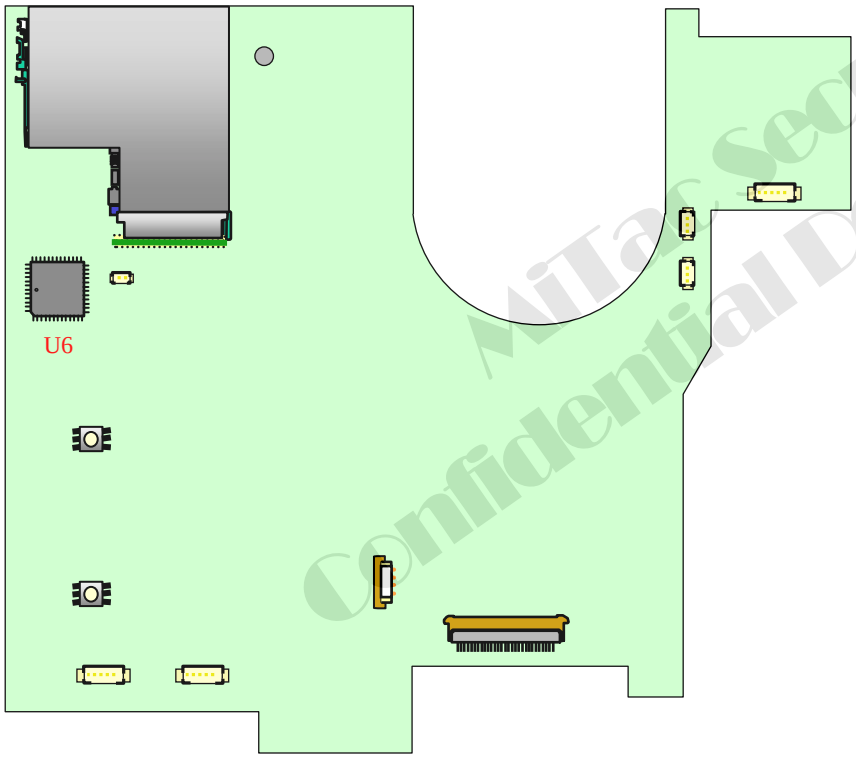
- U503 : Intel Yonah Processor
- U506 : Intel 945GM North Bridge
- U510: MDC
- U512: TPS2231 New Card
- U513 : W83L951D Keyboard Controller
- U514 : RTL8100CL LAN Controller
- U515 : Intel ICH7-M South Bridge
- U518 : Audio Codec ALC883

4. Definition & Location of Major Components

4.2 Mother Board (Side B)



- U6 : System BIOS

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5. Pin Descriptions of Major Components

5.1 Intel Yonah Processor CPU (1)

CPU Pin Description

Signal Name	Type	Description
A[31:3]#	I/O	A[31:]#(Address) define a 2*32- byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. Must connect the appropriate pins of both agents on the Intel Core TM Duo processor and the Intel Core TM Solo processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M#(Address-20 Mask) is asserted, the processor masks physical address bit 20(A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS#(Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[31:17]# — ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

CPU Pin Description (Continued)

Signal Name	Type	Description
BPM[2:1]# **BPM[3,0]#**	I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the Mobile Intel 945 Express chipset family (High Priority Agent).
BSEL[2:0]	O	BSEL[2:0] (Bus SELECT) are used to select the processor input clock frequency. The table defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The processor operates at 667 MHz or 533 MHz system bus frequency (166MHz or 133MHz BCLK[1:0] frequency, respectively). BSE[2:0] Encoding for BCLK Frequency BSEL[2] / BSEL[1] / BSE[0] / BCLK Frequency L / L / L / Reserved L / L / H / 133MHz L / H / L / Reserved L / H / H / 166MHz
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.

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5.1 Intel Yonah Processor CPU (2)

CPU Pin Description (Continued)

Signal Name	Type	Description
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** **Data Group** / **DSTBN#/DSTBP#** / **DINV#** D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.

CPU Pin Description (Continued)

Signal Name	Type	Description
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** **Bus Signal** / **Data Bus Signals** DINV[3]# / D[63:48]# DINV[2]# / D[47:32]# DINV[1]# / D[31:16]# DINV[0]# / D[15:0]#
DPRSTP#	I	DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep Stated. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the Intel ICH7M chipset.
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH7M chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DINV[0]# / DSTBN[0]# D[31:16]#, DINV[1]# / DSTBN[1]# D[47:32]#, DINV[2]# / DSTBN[2]# D[63:48]#, DINV[3]# / DSTBN[3]#

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5.1 Intel Yonah Processor CPU (3)

CPU Pin Description (Continued)

Signal Name	Type	Description
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the Intel Architecture Software Developer's Manual and AP-485, For termination requirements please contact your Intel representative.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 VCCP . GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.Plese contact your Intel representative for more information regarding GTLREF implementation.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.

CPU Pin Description (Continued)

Signal Name	Type	Description
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	I	INIT#(Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers, The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write Instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction, INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Selt-Test(BIST).
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.

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5.1 Intel Yonah Processor CPU (4)

CPU Pin Description (Continued)

Signal Name	Type	Description
LOCK#	I/O	When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	I/O	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. TCC will remain active until the system deasserts PRCCHOT#. By default PROCHOT# is configured as an output only. Bidirectional PROCHOT# must be enabled via the BIOS. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (HFM and LFM) and lower state (Deep Sleep and Deeper Sleep).
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
REQ[4:0]	I/O	REQ[4:0]#(Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications.

CPU Pin Description (Continued)

Signal Name	Type	Description
RESET#	I	On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. There is a 55 (normal) on die pull up resistor on this signal.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.

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5.1 Intel Yonah Processor CPU (5)

CPU Pin Description (Continued)

Signal Name	Type	Description
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1,	I	TEST1 must have a stuffing option of separate pull down resistor to Vss.
TEST2	I	TEST2 must have a 51±5% pull down resistor to Vss.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
Vcc	I	Processor core power supply.
Vcca	I	Vcca provides isolated power for the internal processor core PLL's.
Vccp	I	Processor I/O Power Supply.
VID[6:0]	O	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the pins, or disable itself.

CPU Pin Description (Continued)

Signal Name	Type	Description
Vsssense	O	Vsssense together with Vccsense are voltage feedback signals to IMVP6 that control the 2.1m loadline at the processor die. It should be used to sense ground near the silicon with little noise.

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5.2 Intel 945GM North Bridge (1)

Host Interface Signals

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** HBNR# is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-toinactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**CPU Reset:** The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH7 must provide processor frequency select strap setup and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the ICH7 driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** HDEFER# indicates that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.

Host Interface Signals (Continued)

Signal Name	Type	Description
HDRDY#	I/O GTL+	**Data Ready:** This signal is asserted for each cycle that data is transferred.
HEDRDY#	O GTL+	**Early Data Ready:** This signal indicates that the data phase of a read transaction will start on the bus exactly one common clock after assertion.
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** These signals are driven along with the HD[63:0] signals. They indicate if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8.. **HDINV[x]# Data Bits** HDINV3# HD[63:48] HDINV2# HD[47:32] HDINV1# HD[31:16] HDINV0# HD[15:0]
HA[31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, the HA[31:3]# are inputs. The (G)MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express* initiators. HA[31:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** These signals are the source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.
HD[63:0]#	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HHIT#	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. In addition, HHIT# is driven in conjunction with HHITM# by the target to extend the snoop window.

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5.2 Intel 945GM North Bridge (2)

Host Interface Signals (Continued)

Signal Name	Type	Description
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** These signals are the differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence they are pseudo-differential, and not true differential. **Strobe** **Data** **Bits** HDSTBP3#, HDSTBN3# HD[63:48] HDINV3# HDSTBP2#, HDSTBN2# HD[47:32] HDINV2# HDSTBP1#, HDSTBN1# HD[31:16] HDINV1# HDSTBP0#, HDSTBN0# HD[15:00] HDINV0#
HHITM#	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. In addition, HHITM# is driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic (i.e., no DMI or PCI Express accesses to DRAM are allowed when HLOCK# is asserted by the processor).
HPCREQ#	I GTL+ 2X	**Precharge Request:** The processor provides a "hint" to the (G)MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The (G)MCH uses this information to schedule the read request to memory using the special "AutoPrecharge" attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. HPCREQ# is asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.
HREQ[4:0]#	I/O GTL+ 2X	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half, the signals carry additional information to define the complete transaction type.

Host Interface Signals (Continued)

Signal Name	Type	Description
HTRDY#	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Host Response Status:** These signals indicate the type of response as shown below: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by (G)MCH) 100 = Hard Failure (not driven by (G)MCH) 101 = No data response 110 = Implicit Write back 111 = Normal data response
BSEL[2:0]	I COMS	**Bus Speed Select:** At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.
HRCOMP	I/O COMS	**Host RCOMP:** This signal is used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V_{TT}).
HSCOMP	I/O COMS	**Slew Rate Compensation:** This is the compensation signal for the Host Interface.
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HDVREF	I A	**Host Reference Voltage:** Voltage input for the data, address, and common clock signals of the Host GTL interface.
HACCVREF	I A	**Host Reference Voltage:** Reference voltage input for the Address, and Common clock signals of the Host GTL interface.

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (VTT).

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5.2 Intel 945GM North Bridge (3)

DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Ax and its complement SCLK_Ax# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_A[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_A[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_A#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-1.8 2X	**Data Lines:** The SDQ_A[63:0] signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax bit for every data byte lane.
SDQS_A[7:0]	I/O SSTL-1.8 2X	**Data Strobes:** For DDR2, SDQS_Ax and its complement SDQS_Ax# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.

DDR2 DRAM Channel A Interface (Continued)

Signal Name	Type	Description
SDQS_A[7:0]#	I/O SSTL-1.8 2X	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Ax is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Bx and its complement SCLK_Bx# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_B[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_B[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_B[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_B#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.

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5.2 Intel 945GM North Bridge (4)

DDR2 DRAM Channel B Interface (Continued)

Signal Name	Type	Description
SCAS_B#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-1.8 2X	**Data Lines:** The SDQ_B[63:0] signals interface to the SDRAM data bus.
SDM_B[7:0]	O SSTL-1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx bit for every data byte lane.
SDQS_B[7:0]	I/O SSTL-1.8 2X	**Data Strobes:** For DDR2, SDQS_Bx and its complement SDQS_Bx# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[7:0]#	I/O SSTL-1.8 2X	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_B[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Bx is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

PCI Express* Interface Signals

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I/O PCIE	**PCI Express* Receive Differential Pair**
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	**PCI Express* Transmit Differential Pair**
EXP_ICOMPO	I A	**PCI Express* Output Current and Resistance Compensation**
EXP_COMPI	I A	**PCI Express* Input Current Compensation**

Unless otherwise specified, PCI Express signals are AC coupled, so the only voltage specified is a maximum 1.2 V differential swing.

Analog Display Signals (Intel® 82945G GMCH Only)

Signal Name	Type	Description
RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
RED#	O A	**REDB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance: however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 ΩCRT load).
GREEN#	O A	**GREENB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
BLUE#	O A	**BLUEB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
REFSET	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 Ω 1% resistor is required between REFSET and motherboard ground.
HSYNC	O 2.5V CMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”. 2.5 V output.
VSYNC	O 2.5V CMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). 2.5 V output.
DDC_CLK	I/O 2.5V CMOS	**Monitor Control Clock:** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
DDC_DATA	I/O 2.5V CMOS	**Monitor Control Data:** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

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5.2 Intel 945GM North Bridge (5)

Clock, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I HCSL	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Memory domain clocks are also derived from this source.
GCLKP GCLKN	I HCSL	**Differential PCI Express* Clock In:** These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I HCSL	**Display PLL Differential Clock In**
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH7. All PCI Express graphics attach output signals will also tri-state compliant to *PCI Express* Specification, Revision 1.0a*. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
EXTTS#	I CMOS	**External Thermal Sensor Input:** This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.
EXP_EN	I CMOS	**PCI Express SDVO Concurrent Select:** 0 = Only SDVO or PCI Express operational 1 = SDVO and PCI Express operating simultaneously via PCI Express port **NOTES:** For the 82945P MCH, this signal should be pulled low.
EXP_SLR	I CMOS	**PCI Express* Lane Reversal/Form Factor Selection:** (G)MCH's PCI Express lane numbers are reversed to differentiate Balanced Technology Extended (BTX) or ATX form factors. 0 = (G)MCH's PCI Express lane numbers are reversed (BTX Platforms) 1 = Normal operation (ATX Platforms)
ICH_SYNC#	O HVCMOS	**ICH Sync:** This signal is connected to the MCH_SYNCH# signal on the ICH7.

Clock, Reset, and Miscellaneous (Continued)

Signal Name	Type	Description
XORTEST	I/O GTL+	**XOR Test:** This signal is used for Bed of Nails testing by OEMs to execute XOR Chain test.
LLLZTEST	I/O GTL+	**All Z Test:** As an input this signal is used for Bed of Nails testing by OEMs to execute XOR Chain test. It is used as an output for XOR chain testing.

DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[1:0]	I/O	**System Memory RCOMP**
SOCOMP[1:0]	I/O A	**DDR2 On-Die DRAM Over Current Detection (OCD) Driver Compensation**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** These signals are reference voltage inputs for each SDQ_x, SDM_x, SDQS_x, and SDQS_x# input signals.

Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I/O DMI	**Direct Media Interface:** These signals are receive differential pairs (Rx).
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** These signals are transmit differential pairs (Tx).

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5.2 Intel 945GM North Bridge (6)

Intel® Serial DVO (SDVO) Interface (Intel® 82945G GMCH Only)

Signal Name	Type	Description
SDVOB_CLK-	O PCIE	**Serial Digital Video Channel B Clock Complement:** This signal is multiplexed with EXP_TXN12.
SDVOB_CLK+	O PCIE	**Serial Digital Video Channel B Clock Clock:** This signal is multiplexed with EXP_TXP12.
SDVOB_RED-	O PCIE	**Serial Digital Video Channel C Red Complement:** This signal is multiplexed with EXP_TXN15.
SDVOB_RED+	O PCIE	**Serial Digital Video Channel C Red:** This signal is multiplexed with EXP_TXP15.
SDVOB_GREEN-	O PCIE	**Serial Digital Video Channel B Green Complement:** This signal is multiplexed with EXP_TXN14.
SDVOB_GREEN+	O PCIE	**Serial Digital Video Channel B Green:** This signal is multiplexed with EXP_TXP14.
SDVOB_BLUE-	O PCIE	**Serial Digital Video Channel B Blue Complement:** This signal is multiplexed with EXP_TXN13.
SDVOB_BLUE+	O PCIE	**Serial Digital Video Channel B Blue:** This signal is multiplexed with EXP_TXP13.
SDVOC_RED-/ SDVOB_ALPHA-	O PCIE	**Serial Digital Video Channel C Red Complement Channel B Alpha Complement:** This signal is multiplexed with EXP_TXN11.
SDVOC_RED+/ SDVOB_ALPHA+	O PCIE	**Serial Digital Video Channel C Red Complement Channel B Alpha:** This signal is multiplexed with EXP_TXP11.
SDVOC_GREEN-	O PCIE	**Serial Digital Video Channel C Green Complement:** This signal is multiplexed with EXP_TXN10.
SDVOC_GREEN+	O PCIE	**Serial Digital Video Channel C Green:** This signal is multiplexed with EXP_TXP10.
SDVOC_BLUE-	O PCIE	**Serial Digital Video Channel C Blue Complement:** This signal is multiplexed with EXP_TXN9.
SDVOC_BLUE+	O PCIE	**Serial Digital Video Channel C Blue:** This signal is multiplexed with EXP_TXP9.
SDVOC_CLK-	O PCIE	**Serial Digital Video Channel C Clock Complement:** This signal is multiplexed with EXP_TXN8.
SDVOC_CLK+	O PCIE	**Serial Digital Video Channel C Clock:** This signal is multiplexed with EXP_TXP8.
SDVO_TVCLKIN-	I PCIE	**Serial Digital Video TV-OUT Synchronization Clock Complement:** This signal is multiplexed with EXP_RXN15.
SDVO_TVCLKIN+	I PCIE	**Serial Digital Video TV-OUT Synchronization Clock:** This signal is multiplexed with EXP_RXP15.
SDVOB_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement:** This signal is multiplexed with EXP_RXN14.

Intel® Serial DVO (SDVO) Interface (Intel® 82945G GMCH Only) (Continued)

Signal Name	Voltage	Description
SDVOB_INT+	I PCIE	**Serial Digital Video Input Interrupt:** This signal is multiplexed with EXP_RXP14.
SDVOC_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement:** This signal is multiplexed with EXP_RXN10.
SDVOC_INT+	I PCIE	**Serial Digital Video Input Interrupt:** This signal is multiplexed with EXP_RXP10.
SDVO_STALL-	I PCIE	**Serial Digital Video Filed Stall Complement:** This signal is multiplexed with EXP_RXN13.
SDVO_STALL+	I PCIE	**Serial Digital Video Filed Stall:** This signal is multiplexed with EXP_RXP13.
SDVO_CTRLCLK	I/O COD	**Serial Digital Video Device Control Clock.**
SDVO_CTRLDATA	I/O COD	**Serial Digital Video Device Control Data.**

Power and Ground

Name	Voltage	Description
VCC	1.5V	Core Power
VTT	1.2V	Processor System Bus Power
VCC_EXP	1.5V	PCI Express* and DMI Power
VCCSM	1.8V	System Memory Power
VCC2	2.5V	2.5V COMS Power
VCCA_EXPPLL	1.5V	PCI Express PLL Analog Power
VCCA_DPLLA (GMCH ONLY)	1.5V	Display PLL A Analog Power
VCCA_DPLLB (GMCH ONLY)	1.5V	Display PLL B Analog Power
VCCA_HPLL	1.5V	Host PLL Analog Power
VCCA_SMPLL	1.5V	System Memory PLL Analog Power
VCCA_DAC	2.5V	Display DAC Analog Power
VSS	0V	Ground
VSSA_DAC	0V	Ground

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5.3 Intel ICH7-M South Bridge (1)

PCI Interface Signals

Signal Name	Type	Description
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH7's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH7 has valid data present on AD[31:0]. During a read, it indicates the ICH7 is prepared to latch data. IRDY# is an input to the ICH7 when the ICH7 is the target and an output from the ICH7 when the ICH7 is an initiator. IRDY# remains tri-stated by the ICH7 until driven by an initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the Intel® ICH7's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH7, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH7, as a target is prepared to latch data. TRDY# is an input to the ICH7 when the ICH7 is the initiator and an output from the ICH7 when the ICH7 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH7 until driven by a target.
STOP#	I/O	**Stop:** STOP# indicates that the ICH7, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH7, as an initiator, to stop the current transaction. STOP# is an output when the ICH7 is a target and an input when the ICH7 is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH7 counts the number of one within the 36 bits plus PAR and the sum is always even. The ICH7 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH7 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH7 drives and tristates PAR identically to the AD[31:0] lines except that the ICH7 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH7 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH7 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH7 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH7 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel® ICH7 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH7 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH7 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH7 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH7 address or an address destined DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH7-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH7 until driven by a target device.
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH7 when the ICH7 is the target, and FRAME# is an output from the ICH7 when the ICH7 is the initiator. FRAME# remains tristated by the ICH7 until driven by an initiator.

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5.3 Intel ICH7-M South Bridge (2)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH7 drives PERR# when it detects a parity error. The ICH7 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[0:3]# **REQ[4]#/** GPIO22 **REQ[5]#**/GPIO1	I	**PCI Requests:** The ICH7 supports up to 6 masters on the PCI bus. The REQ[4]# and REQ5# pins can instead be used as a GPIO.
GNT[0:3]# **GNT[4]#/** GPIO48 **GNT[5]#/** GPIO17#	O	**PCI Grants:** The ICH7 supports up to 6 masters on the PCI bus. The GNT4# and GNT5# pins can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT5#/GPIO17 has an internal pull-up.
PCICLK	I	**NOTE: PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus.
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. The ICH7 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus in desktop configurations.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH7 has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH7 may drive PME# active due to an internal wake event. The ICH7 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

Serial ATA Interface Signals

Name	Type	Description
SATA0TXP **SATA0TXN**	O	**Serial ATA 0 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 0.
SATA0RXP **SATA0RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0.
SATA1TXP **SATA1TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1.
SATA1RXP **SATA1RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1.
SATA2TXP **SATA2TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2.
SATA2RXP **SATA2RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2.
SATA3TXP **SATA3TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3.
SATA3RXP **SATA3RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3.
SATARBIAS	O	**Serial ATA Resistor Bias:** These are analog connection points for an external resistor to ground.
SATARBIAS#	I	**Serial ATA Resistor Bias Complement:** These are analog connection points for an external resistor to ground.
SATA0GP/ GPIO21	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP/ GPIO19	I	**Serial ATA 1 General Purpose:** Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP/ GPIO36	I	**Serial ATA 2 General Purpose:** Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36.

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5.3 Intel ICH7-M South Bridge (3)

Serial ATA Interface Signals (Continued)

Name	Type	Description
SATA3GP/ GPIO37	I	**Serial ATA 3 General Purpose:** Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37.
SATALED#	OC	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. **NOTE:** An internal pull-up is enabled only during PLTRST# assertion.
SATACLKREQ #/GPIO35	OD (Native)/ I/O (GP)	**Serial ATA Clock Request:** This is an open-drain output pin when configured as SATACLKREQ#. It is to connect to the system clock chip. When active, request for SATA Clock running is asserted. When tri-stated, it tells the Clock Chip that SATA Clock can be stopped. An external pull-up resistor is required.

Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS#	I/O	**SPI Chip Select:** Also used as the SPI bus request signal.
SPI_MISO	I	**SPI Master IN Slave OUT:** Data input pin for Intel® ICH7.
SPI_MOSI	O	**SPI Master OUT Slave IN:** Data output pin for ICH7.
SPI _ARB	I	**SPI Arbitration:** SPI arbitration signal is used to arbitrate the SPI bus with Intel PRO 82573E Gigabit Ethernet Controller when Shared Flash is implemented.
SPI_CLK	O	**SPI Clock:** SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz.

Platform LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** This signal is driven by the Platform LAN Connect component. The frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The Platform LAN Connect component uses these signals to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data:** The integrated LAN controller uses these signals to transfer data and control information to the Platform LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The Platform LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

Other Clock

Name	Type	Description
CLK14	I	**Oscillator Clock:** This clock is used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. Runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the SATA controller at 100 MHz. This clock is permitted to stop during S3/S4/S5 states.
DMI_CLKP, DMI_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the Direct Media Interface. Runs at 100 MHz.

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5.3 Intel ICH7-M South Bridge (4)

IDE Interface Signals

Name	Type	Description
DCS1#	O	**IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the IDE connector.
DCS3#	O	**IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the IDE connector.
DA[2:0]	O	**IDE Device Address:** These output signals are connected to the corresponding signals on the IDE connector. They are used to indicate which byte in either the ATA command block or control block is being addressed.
DD[15:0]	I/O	**IDE Device Data:** These signals directly drive the corresponding signals on the IDE connector. There is a weak internal pull-down resistor on DD7.
DDREQ	I	**IDE Device DMA Request:** This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pulldown resistor on this signal.
DDACK#	O	**IDE Device DMA Acknowledge:** This signal directly drives the DAK# signal on the IDE connector. DDACK# is asserted by the Intel® ICH7 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
DIOR#/ (DWSTB/ RDMARDY#)	O	**DIOR# /Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the DD lines. Data is latched by the ICH7 on the deassertion edge of DIOR#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH7 drives valid data on rising and falling edges of DWSTB. Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH7 deasserts RDMARDY# to pause burst data transfers.

IDE Interface Signals (Continued)

Name	Type	Description
DIOW#/ (DSTOP)	O	**Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the DD lines. Data is latched by the IDE device on the deassertion edge of DIOW#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Stop (Ultra DMA): ICH7 asserts this signal to terminate a burst.
IORDY/ (DRSTB/ WDMARDY#)	I	**I/O Channel Ready (PIO):** This signal will keep the strobe active (DIOR# on reads, DIOW# on writes) longer than the minimum width. It adds wait-states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, ICH7 latches data on rising and falling edges of this signal from the disk. Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is deasserted by the disk to pause burst data transfers.

System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPIO if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT#	I/OD	**SMLink Alert:** Output of the integrated LAN and input to either the integrated ASF or an external management controller in order for the LAN's SMLINK slave to be serviced.

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5.3 Intel ICH7-M South Bridge (5)

USB Interface Signals

Name	Type	Description
USBP0P, **USBP0N,** **USBP1P,** **USBP1N**	I/O	**Universal Serial Bus Port [1:0] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The Intel® ICH7 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, **USBP2N,** **USBP3P,** **USBP3N**	I/O	**Universal Serial Bus Port [3:2] Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH7 integrates 15 KΩ ?pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, **USBP4N,** **USBP5P,** **USBP5N**	I/O	**Universal Serial Bus Port [5:4] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH7 integrates 15 KΩ ?pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP6P, **USBP6N,** **USBP7P,** **USBP7N**	I/O	**Universal Serial Bus Port [7:6] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH7 integrates 15 KΩ ?pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
OC[4:0]# **OC5#**/GPIO29 **OC6#**/GPIO30 **OC7#**/GPIO31	I	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:4]# may optionally be used as GPIOs. **NOTE:** OC[7:0]# are not 5 V tolerant.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock:** Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In:** Transfers data from the EEPROM to the Intel® ICH7. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out:** Transfers data from the ICH7 to the EEPROM.
EE_CS	O	**EEPROM Chip Select:** Chip select signal to the EEPROM.

Interrupt Signals

Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the *Interrupt Steering* section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IDEIRQ	I	**IDE Interrupt Request:** This interrupt input is connected to the IDE drive.

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5.3 Intel ICH7-M South Bridge (6)

Power Management Interface Signals

Name	Type	Description
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pullup resistor and has an internal 16 ms de-bounce on the input.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH7 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller will be put into reset. This signal must be asserted for at least 10 ms after the resume well power (VccSus3_3 and VccSus1_5) is valid. When de-asserted, this signal is an indication that the resume well power is stable. **NOTE:** LAN_RST# should be tied to RSMEST#.
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wakeup.
MCH_SYNC#	I	**MCH SYNC:** This input is internally ANDed with the PWROK input. Connected to the ICH_SYNC# output of (G)MCH.
THRM#	I	**Thermal Alarm:** Active low signal generated by external hardware to generate an SMI# or SCI.
THRMTRIP#	I	**Thermal Trip:** When low, this signal indicates that a thermal trip from the processor occurred, and the ICH7 will immediately transition to a S5 state. The ICH7 will not wait for the processor stop grant cycle since the processor has overheated.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH7 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.

Power Management Interface Signals (Continued)

Name	Type	Description
SUSCLK	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.
VRMPWRGD	I	**VRM Power Good:** This should be connected to be the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input.
PLTRST#	O	**Platform Reset:** The Intel® ICH7 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, IDE, TPM, etc.). The ICH7 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH7 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH7 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the VccSus3_3 well.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power to use the ICH7's DRAM power-cycling feature. Refer to Chapter 5.14.10.2 for details.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH7 that core power has been stable for 99 ms and that PCICLK has been stable for 1 ms. An exception to this rule is if the system is in S3HOT, in which PWROK may or may not stay asserted even though PCICLK may be inactive. PWROK can be driven asynchronously. When PWROK is negated, the ICH7 asserts PLTRST#. **NOTE:** PWROK must deassert for a minimum of three RTC clock periods for the ICH7 to fully reset the power and properly generate the PLTRST# output.

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5.3 Intel ICH7-M South Bridge (7)

Processor Interface Signals

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The Intel® ICH7 can optionally assert the CPUSLP# signal when going to the S1 state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH7 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is asserted, the ICH7 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH7 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor. Error register is written, the IGNNE# signal is not asserted.
INIT#	O	**Initialization:** INIT# is asserted by the ICH7 for 16 PCI clocks to reset the processor. ICH7 can be configured to support processor Built In Self Test (BIST).
INIT3_3V#	O	**Initialization 3.3 V:** This is the identical 3.3 V copy of INIT# intended for Firmware Hub.
INTR	O	**Processor Interrupt:** INTR is asserted by the ICH7 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.

Processor Interface Signals (Continued)

Name	Type	Description
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH7 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH7 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH7 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH7's other sources of INIT#. When the ICH7 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH7 will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD/ GPIO49	O	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input to indicate when the CPU power is valid. This is an output signal that represents a logical AND of the ICH7's PWROK and VRMPWRGD signals. This signal may optionally be configured as a GPIO.

Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals:** These signals are multiplexed with the LPC address signals.
FWH4/ LFRAME#	O	**Firmware Hub Signals:** This signal is multiplexed with the LPC LFRAME# signal.

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5.3 Intel ICH7-M South Bridge (8)

General Purpose I/O Signals

Name	Type	Tolerance	Power Well	Description
GPIO49	I/O	V_CPU_IO	V_CPU_IO	Multiplexed with CPUPWRGD
GPIO48	I/O	3.3 V	Core	Multiplexed with GNT4#
GPIO[47:40]	N/A	3.3 V	N/A	Not implemented.
GPIO[39:38]	I/O	3.3 V	Core	Unmultiplexed.
GPIO37	I/O	3.3 V	Core	Multiplexed with SATA3GP.
GPIO36	I/O	3.3 V	Core	Multiplexed with SATA2GP.
GPIO35	I/O	3.3 V	Core	Multiplexed with SATACLKREQ#.
GPIO34	I/O	3.3 V	Core	Unmultiplexed.
GPIO33	I/O	3.3 V	Core	Unmultiplexed.
GPIO32	I/O	3.3 V	Core	Unmultiplexed.
GPIO31	I/O	3.3 V	Resume	Multiplexed with OC7#
GPIO30	I/O	3.3 V	Resume	Multiplexed with OC6#
GPIO29	I/O	3.3 V	Resume	Multiplexed with OC5#
GPIO28	I/O	3.3 V	Resume	Unmultiplexed.
GPIO27	I/O	3.3 V	Resume	Unmultiplexed.
GPIO26	I/O	3.3 V	Resume	Unmultiplexed.
GPIO25	I/O	3.3 V	Resume	Unmultiplexed.
GPIO24	I/O	3.3 V	Resume	Unmultiplexed. Not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Multiplexed with LDRQ1#
GPIO22	I/O	3.3 V	Core	Multiplexed with REQ4#
GPIO21	I/O	3.3 V	Core	Multiplexed with SATA0GP.
GPIO20	I/O	3.3 V	Core	Unmultiplexed.
GPIO19	I/O	3.3 V	Core	Multiplexed with SATA1GP.
GPIO18	I/O	3.3 V	Core	Unmultiplexed.
GPIO17	I/O	3.3 V	Core	Multiplexed with GNT5#.
GPIO16	I/O	3.3 V	Core	Unmultiplexed.
GPIO[15:12]	I/O	3.3 V	Resume	Unmultiplexed.
GPIO11	I/O	3.3 V	Resume	Multiplexed with SMBALERT#
GPIO[10:8]	I/O	3.3 V	Resume	Unmultiplexed.
GPIO[7:6]	I/O	3.3 V	Core	Unmultiplexed.
GPIO[5:2]	I/OD	5 V	Core	Multiplexed with PIRQ[H:E]#.

General Purpose I/O Signals (Continued)

Name	Type	Tolerance	Power Well	Description
GPIO1	I/O	5 V	Core	Multiplexed with REQ5#.
GPIO0	I/O	3.3 V	Core	Unmultiplexed.

NOTES:

1. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.
2. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some ICH7 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH7 driving a pin to a logic 1 to another device that is powered down..

PCI Express* Signals

Name	Type	Description
PETp[1:4], PETn[1:4]	O	**PCI Express* Differential Transmit Pair 1:4**
PERp[1:4], PERn[1:4]	I	**PCI Express Differential Receive Pair 1:4**
PETp[5:6], PETn[5:6] (Intel® ICH7R Only)	O	**PCI Express* Differential Transmit Pair 5:6 Reserved: ICH7**
PERp[1:4], PERn[5:6] (ICH7R Only)	I	**PCI Express Differential Receive Pair 5:6 Reserved: ICH7**

SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up resistor is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up resistor is required.
SMBALERT#/ GPIO11	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPIO.

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5.3 Intel ICH7-M South Bridge (9)

AC'97/Intel® High Definition Auto Link Signals

Name	Type	Description
ACZ_RST#	O	**AC'97/Intel® High Definition Audio Reset:** Master hardware reset to external codec(s).
ACZ_SYNC	O	**AC '97/Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number.
ACZ_BIT_CLK	I/O	**AC '97 Bit Clock Input:** 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor (see Note below). **Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the Intel® ICH7). This signal has an integrated pull-down resistor so that ACZ_BIT_CLK doesn't float when an Intel High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC '97.
ACZ_SDOUT	O	**AC '97/Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. **NOTE:** ACZ_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Function Straps for more details. There is a weak integrated pull-down resistor on the ACZ_SDOUT pin.
ACZ_SDIN[2:0]	I	**AC '97/Intel High Definition Audio Serial Data In [2:0]:** Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio. These signals have integrated pulldown resistors, which are always enabled.

LPC Interface Signals

Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME#/ FWH4	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[0]# LDRQ[1]#/ GPIO23	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

Power and Ground Signals

Name	Description
Vcc3_3	3.3 V supply for core well I/O buffers (22 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_05	1.05 V supply for core well logic (20 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for Logic and I/O (30 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for Logic and I/O (53 pins). This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs (2 pins). This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3.3 V supply for resume well I/O buffers (24 pins). This power is not expected to be shut off unless the system is unplugged in desktop configurations.
VccSus1_05	1.05 V supply for resume well logic (5 pins). This power is not expected to be shut off unless the system is unplugged in desktop configurations. This voltage may be generated internally (see Function Straps for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF_Sus	Reference for 5 V tolerance on resume well inputs (1 pin). This power is not expected to be shut off unless the system is unplugged in desktop configurations.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well (1 pin). This power is not expected to be shut off unless the RTC battery is removed or completely drained. **Note:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Intel® ICH7-based platform can be done by using a jumper on RTCRST# or GPI.
VccUSBPLL	1.5 V supply for core well logic (1 pin). This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if USB not used.
VccDMIPLL	1.5 V supply for core well logic (1 pins. This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.
VccSATAPLL	1.5 V supply for core well logic (1 pins). This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if SATA not used.
V_CPU_IO	Powered by the same supply as the processor I/O voltage (3 pins). This supply is used to drive the processor interface signals listed in Process Interface Signals.
Vss	Grounds (194 pins).

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5.3 Intel ICH7-M South Bridge (10)

Functional Strap Definitions

Signal	Usage	When Sampled	Description
GNT3#	Top-Block Swap Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (Intel® ICH7 inverts A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT2#	Reserved		This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
REQ[4:1]#	XOR Chain Selection	Rising Edge of PWROK	See Chapter 25 for functionality information.
LINKALERT#	Reserved		This signal requires an external pull-up resistor.
SPKR	No Reboot	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (ICH7 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
INTVRMEN	Integrated VccSus1_05 VRM Enable/ Disable	Always	Enables integrated VccSus1_05 VRM when sampled high.
EE_CS	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
EE_DOUT	Reserved		This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection	Rising Edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups.Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11:10) (GNT5# is MSB) 01-SPI 10-PCI 11-LPC

Functional Strap Definitions (Continued)

Signal	Usage	When Sampled	Description
ACZ_SDOUT	XOR Chain Entrance/PCI Express* Port Config bit 1	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. See Chapter 25 for XOR Chain functionality information. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 7.1.34 for details. This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Port Config bit 0	Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 7.1.34 for details.
GPIO25	Reserved	Rising Edge of RSMRST#	This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
GPIO16	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
SATALED#	Reserved		This signal has a weak internal pull-up enabled only when PLTRST# is asserted. **NOTE:** This signal should not be pulled low.
TP3	XOR Chain Entrance	Rising Edge of PWROK	See Chapter 25 for functionality information. This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low unless using XOR Chain testing.

Direct Media Interface Signals

Name	Type	Description
DMI[0:3]TXP, DMI[0:3]TXN	O	**Direct Media Interface Differential Transmit Pair 0:3**
DMI[0:3]RXP, DMI[0:3]RXN	I	**Direct Media Interface Differential Receive Pair 0:3**
DMI_ZCOMP	O	**Impedance Compensation Input:** Determines DMI input impedance.
DMI_IRCOMP	I	**Impedance/Compensation Compensation Output:** Determines DMI output impedance and bias current.

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5.3 Intel ICH7-M South Bridge (11)

Miscellaneous Signals

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal 1.05 V Suspend regulator when connected to VccRTC. When connected to Vss, the internal regulator is disabled.
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap. See Function Straps for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. **NOTES:** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
TP0	I	**Test Point 0:** This signal must have an external pull-up to VccSus3_3.
TP1	O	**Test Point 1:** Route signal to a test point.
TP2	O	**Test Point 2:** Route signal to a test point.
TP3	I/O	**Test Point 3:** Route signal to a test point.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX2 should be left floating.

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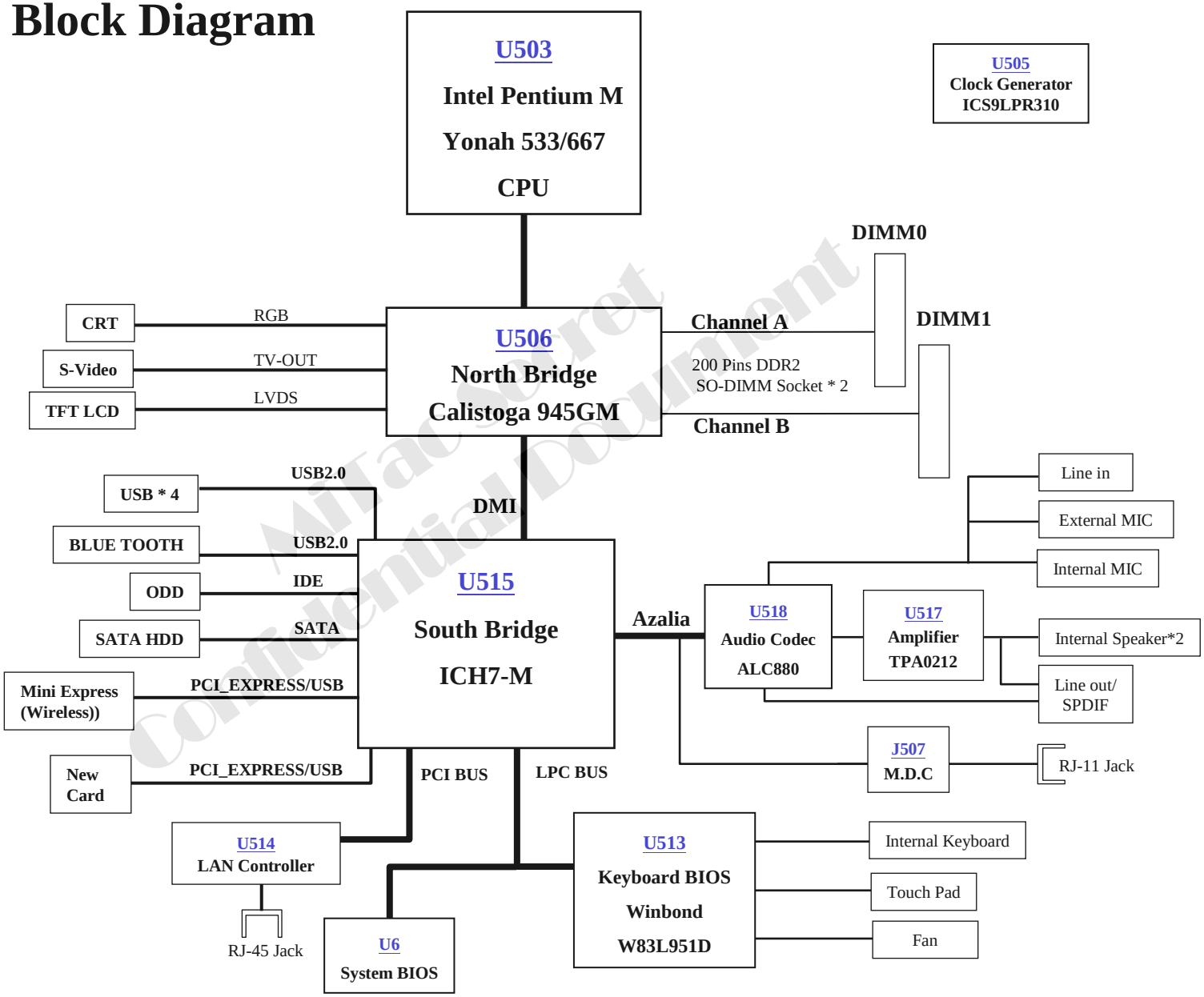
6. System Block Diagram



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7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This Power on Self Test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port-80H by the debug card plug at Mini PCI slot.

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7.2 Maintenance Diagnostics

7.2.1 Diagnostic Tool for Mini PCI-E Slot

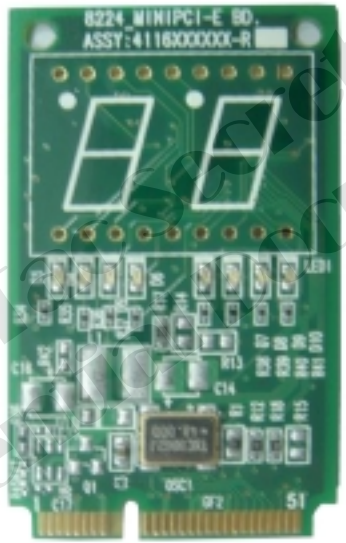

Figure 7-1 PCI-E debug card

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7.3 Error Codes-1

Following is a list of error codes in sequent display on the Mini PCI debug board.

Code	POST Routine Description
10h	Some Type of Lone Reset
11h	Turn off FAST A20 for Post
12h	Signal Power On Reset
13h	Initialize the Chipset
14h	Search for ISA Bus VGA Adapter
15h	Reset Counter / Timer 1
16h	User Register Config through CMOS
17h	Size Memory
18h	Dispatch to RAM Test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize Video Adapter(s)
1Ch	Initialize Video (6845Regs)
1Dh	Initialize Color Adapter
1Eh	Initialize Monochrome Adapter
1Fh	Test 8237A Page Registers

Code	POST Routine Description
20h	Test Keyboard
21h	Test Keyboard Controller
22h	Check if CMOS RAM valid
23h	Test Battery Fail & CMOS X-SUM
24h	Test the DMA Controller
25h	Initialize 8237A Controller
26h	Initialize Int Vectors
27h	RAM Quick Sizing
28h	Protected Mode Entered Safely
29h	RAM Test Completed
2Ah	Protected Mode Exit Successful
2Bh	Setup Shadow
2Ch	Going to Initialize Video
2Dh	Search for Monochrome Adapter
2Eh	Search for Color Adapter
2Fh	Sign on Messages Displayed

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7.3 Error Codes-2

Following is a list of error codes in sequent display on the Mini PCI debug board.

Code	POST Routine Description
30h	Special Init of Keyboard Controller
31h	Test if Keyboard Present
32h	Test Keyboard Interrupt
33h	Test Keyboard Command Byte
34h	Test, Blank and Count all RAM
35h	Protected Mode Entered Safely(2)
36h	RAM Test Complete
37h	Protected Mode Exit Successful
38h	Update Output Port
39h	Setup Cache Controller
3Ah	Test if 18.2Hz Periodic Working
3Bh	Test for RTC ticking
3Ch	Initialize the Hardware Vectors
3Dh	Search and Init the Mouse
3Eh	Update NUMLOCK status
3Fh	Special Init of COMM and LPT Ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the Floppies
42h	Initialize the Hard Disk
43h	Initialize Option ROMs
44h	OEM's Init of Power Management
45h	Update NUMLOCK Status
46h	Test for Coprocessor Installed
47h	OEM functions before Boot
48h	Dispatch to Operate System Boot
49h	Jump into Bootstrap Code

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8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 No Display (*2)
- 8.3 Memory Test Error
- 8.4 Keyboard (K/B) or Touch Pad (T/P) Test Error
- 8.5 Hard Disk Drive Test Error
- 8.6 ODD Test Error
- 8.7 USB Port Test Error
- 8.8 Audio Test Error
- 8.9 LAN Test Error
- 8.10 Mini Express (wireless) Socket Test Error
- 8.11 New Card Socket Test Error

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8258I N/B Maintenance

*1: No Power Definition

Base on ACPI Spec, We define no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display.

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification.

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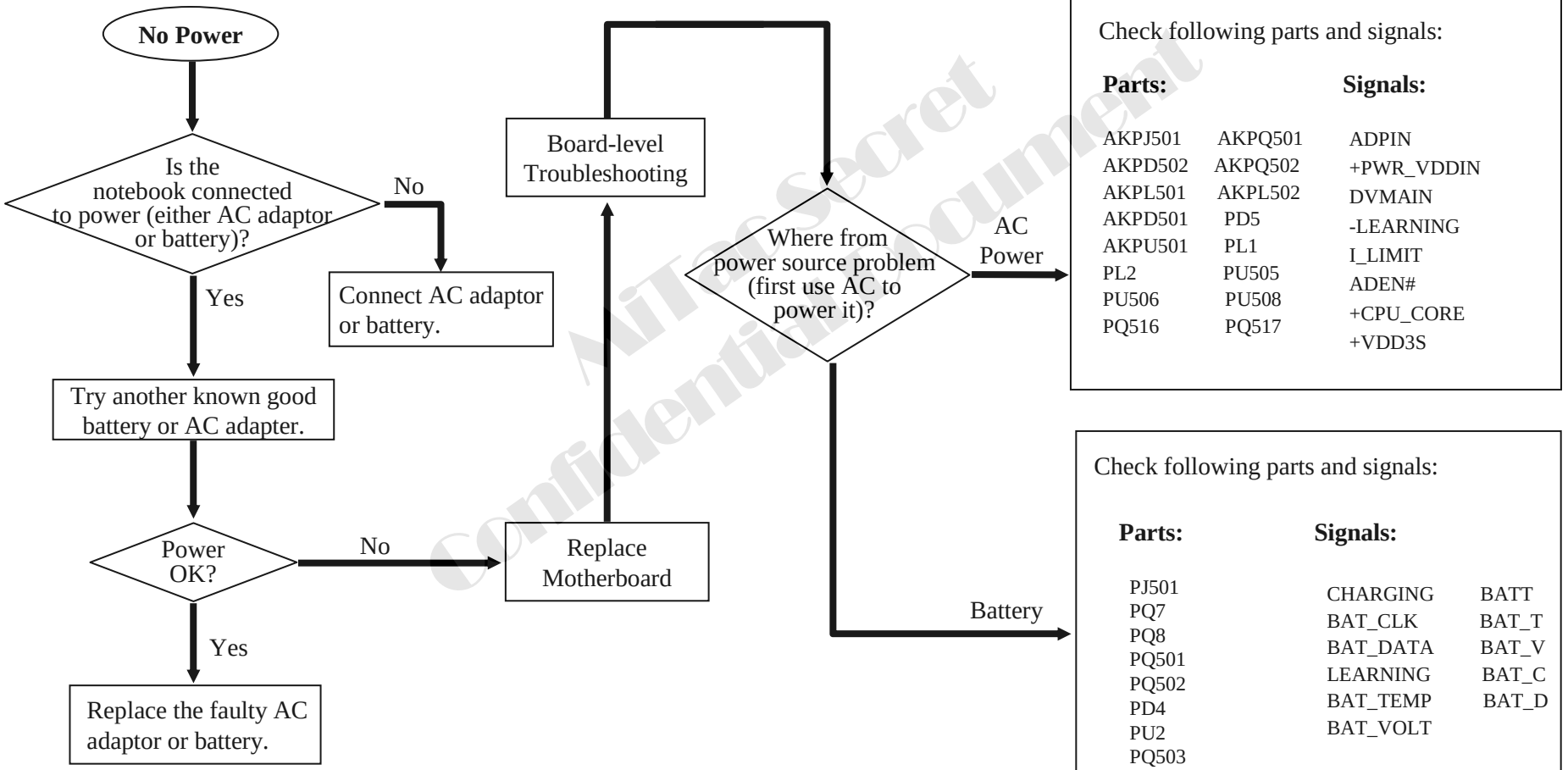
8.1 No Power-1

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

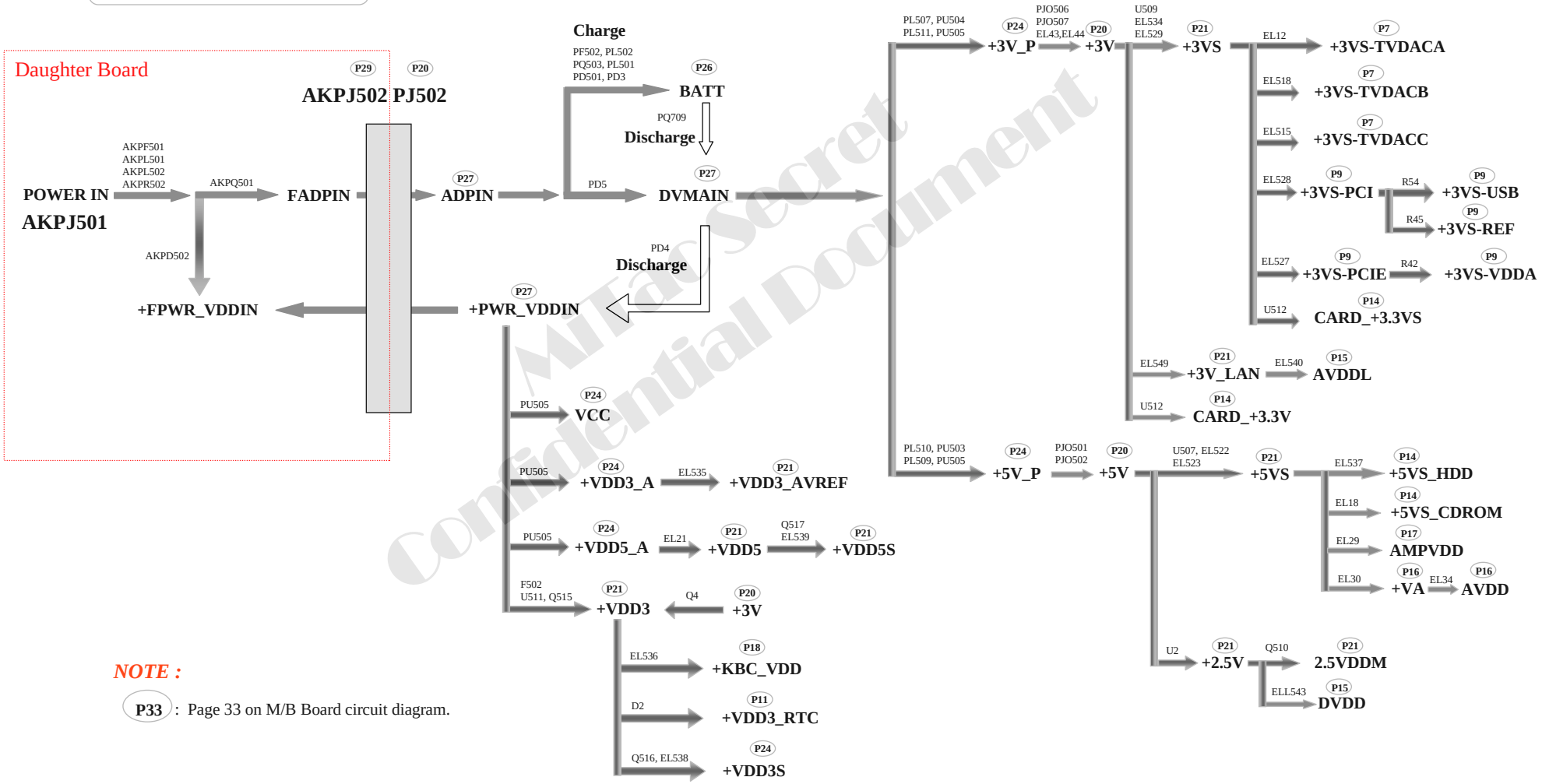


AiTech Secret Confidential Document

8.1 No Power-2

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



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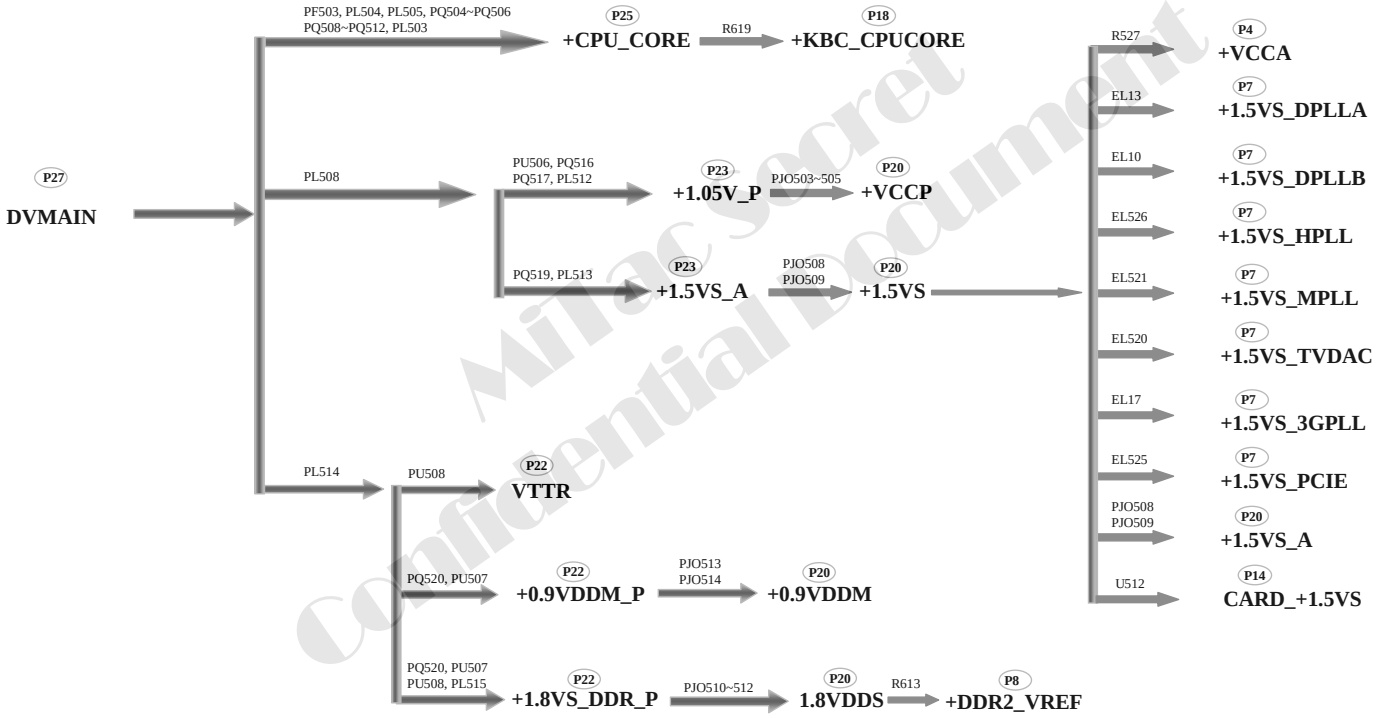
NOTE :

P33 : Page 33 on M/B Board circuit diagram.

8.1 No Power-3

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Continue to the previous page



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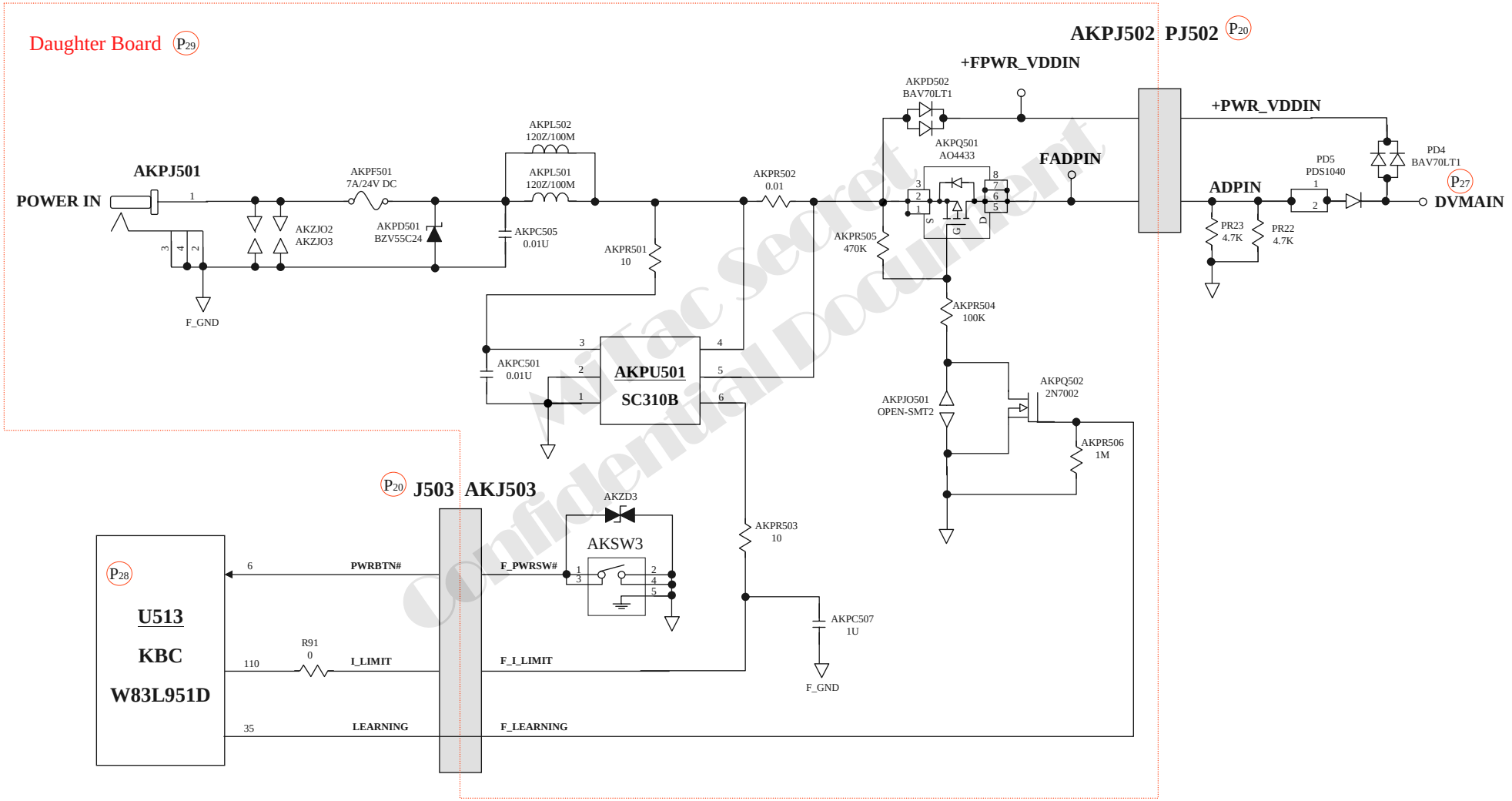
NOTE :

P33 : Page 33 on M/B Board circuit diagram.

8.1 No Power-4

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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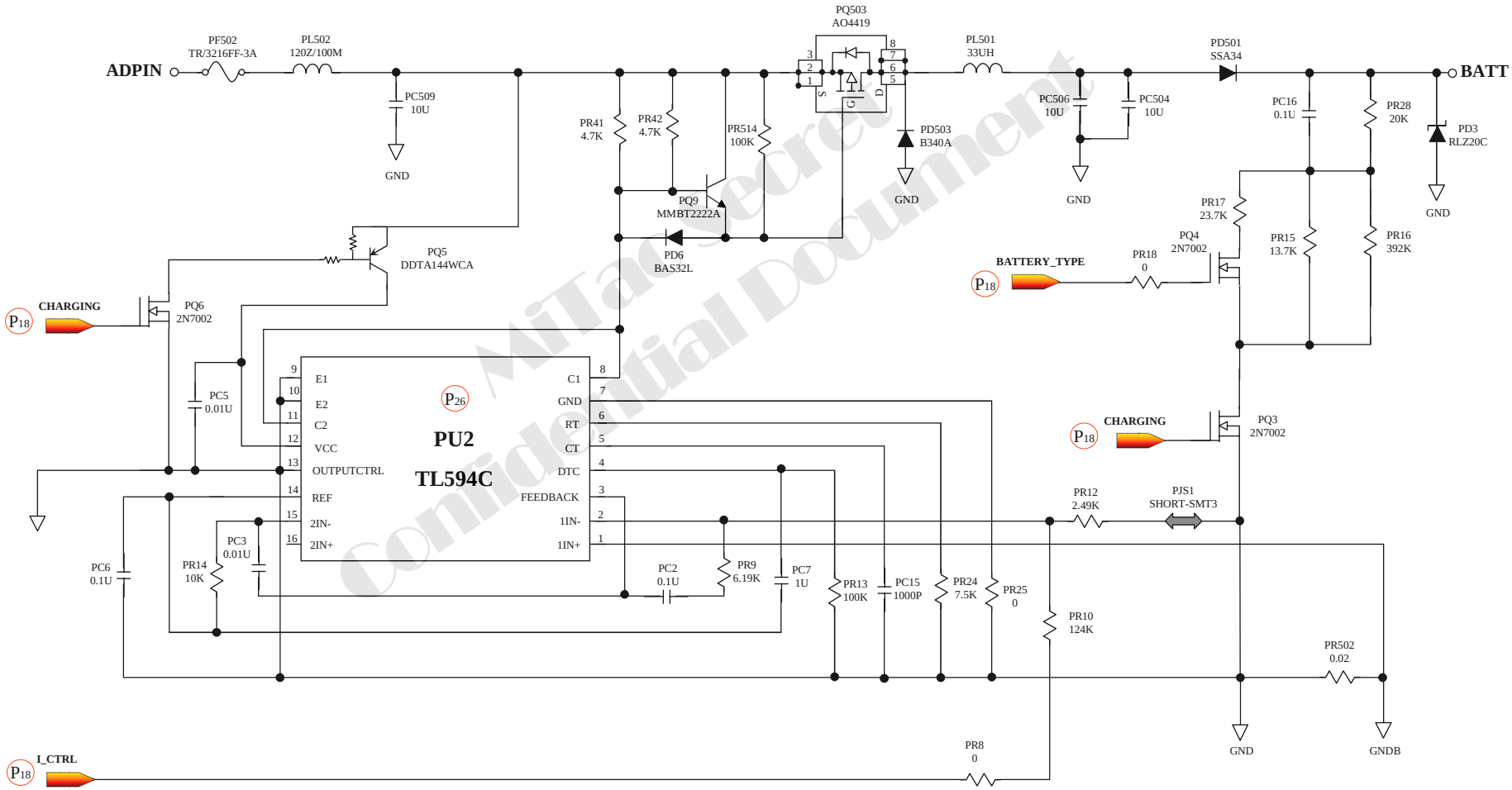
8.1 No Power-5

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Charge



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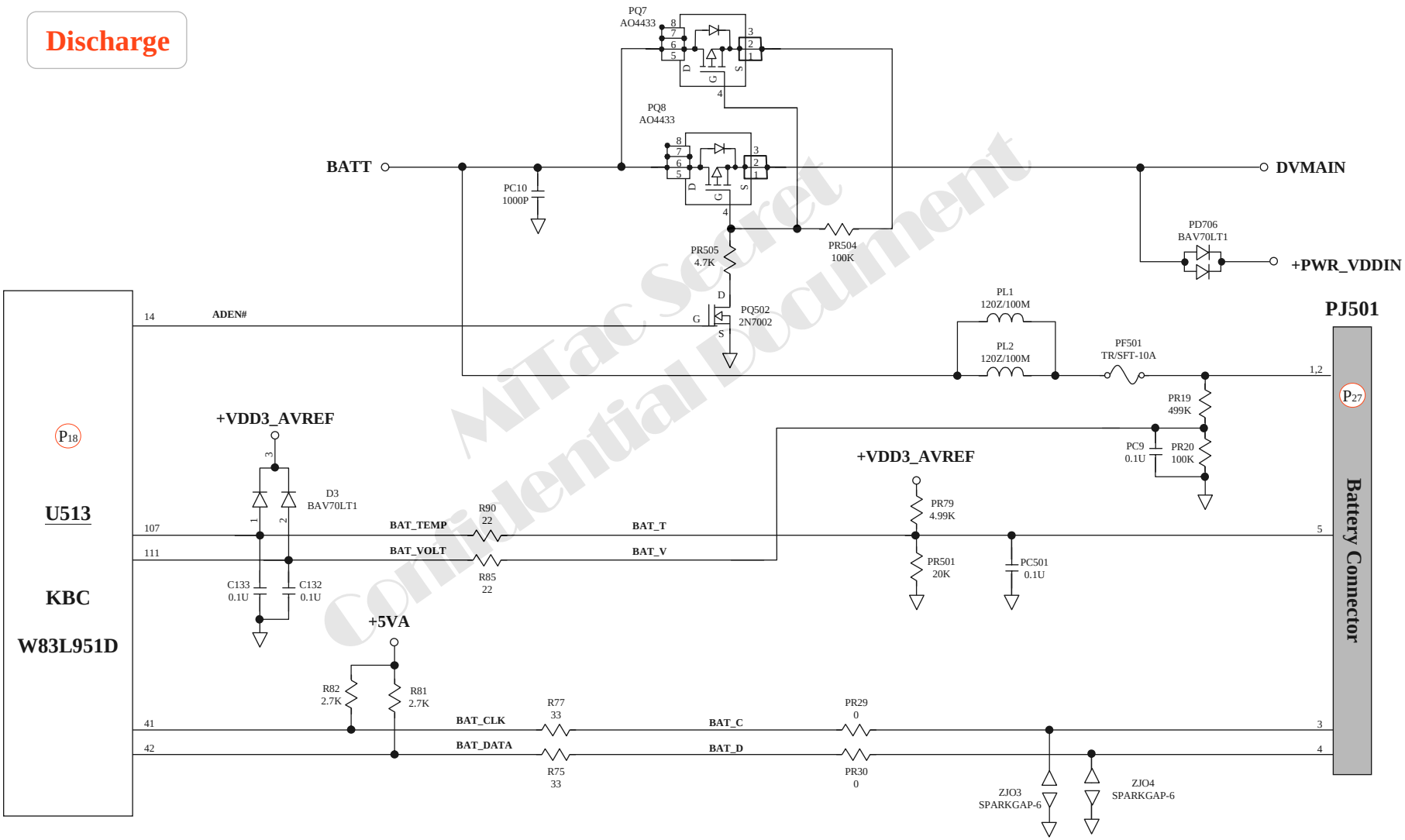
8.1 No Power-6

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Discharge



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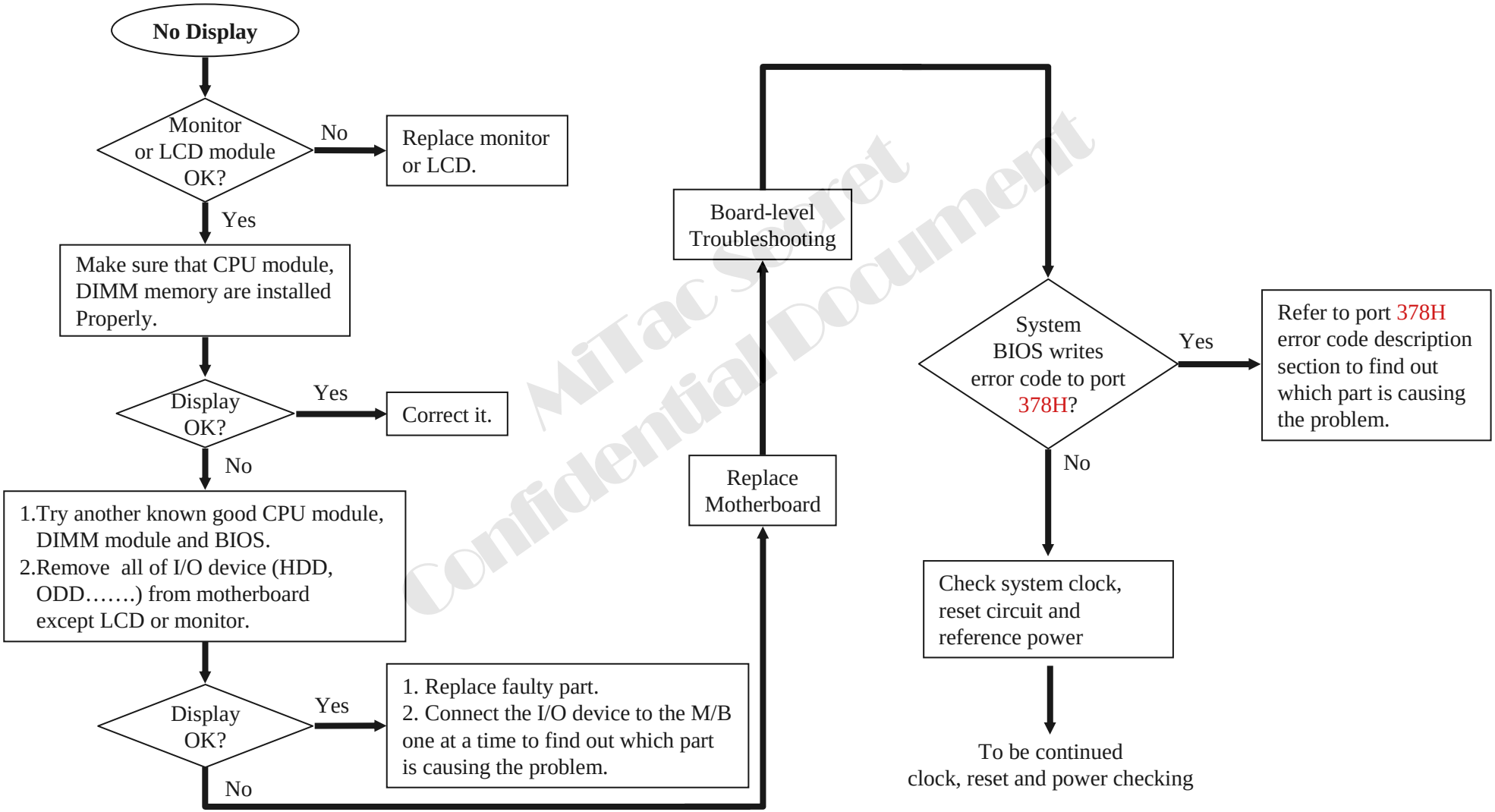
8.2 No Display-1

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.


No Display
Monitor or LCD module OK?
No
Replace monitor or LCD.
Yes
Make sure that CPU module, DIMM memory are installed Properly.
Display OK?
Yes
Correct it.
No
1.Try another known good CPU module, DIMM module and BIOS.
2.Remove all of I/O device (HDD, ODD…….) from motherboard except LCD or monitor.
Display OK?
Yes
1. Replace faulty part.
2. Connect the I/O device to the M/B one at a time to find out which part is causing the problem.
No
Board-level Troubleshooting
Replace Motherboard
System BIOS writes error code to port 378H?
Yes
Refer to port 378H error code description section to find out which part is causing the problem.
No
Check system clock, reset circuit and reference power
To be continued
clock, reset and power checking

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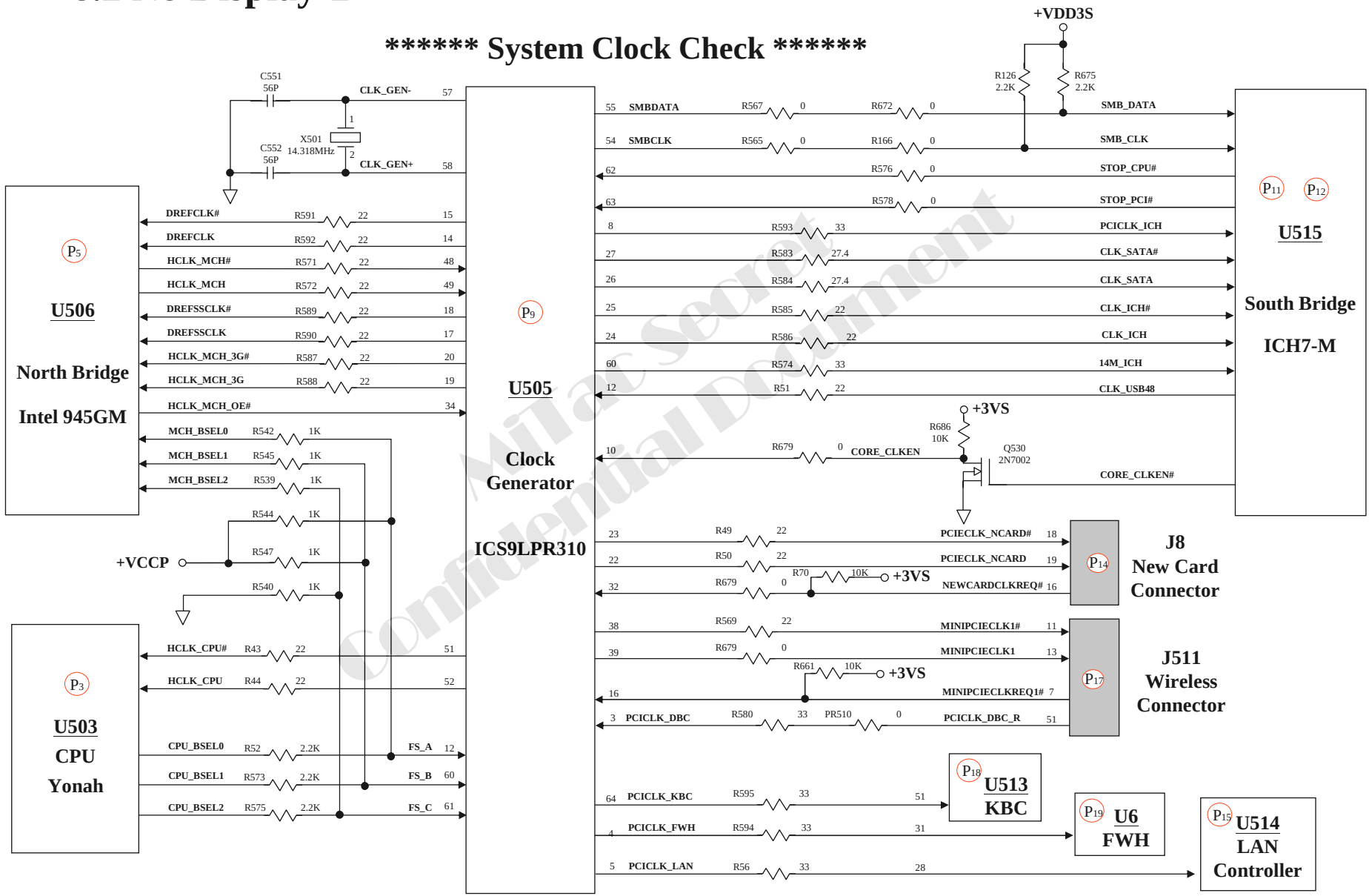
8258I N/B Maintenance

8.2 No Display-2



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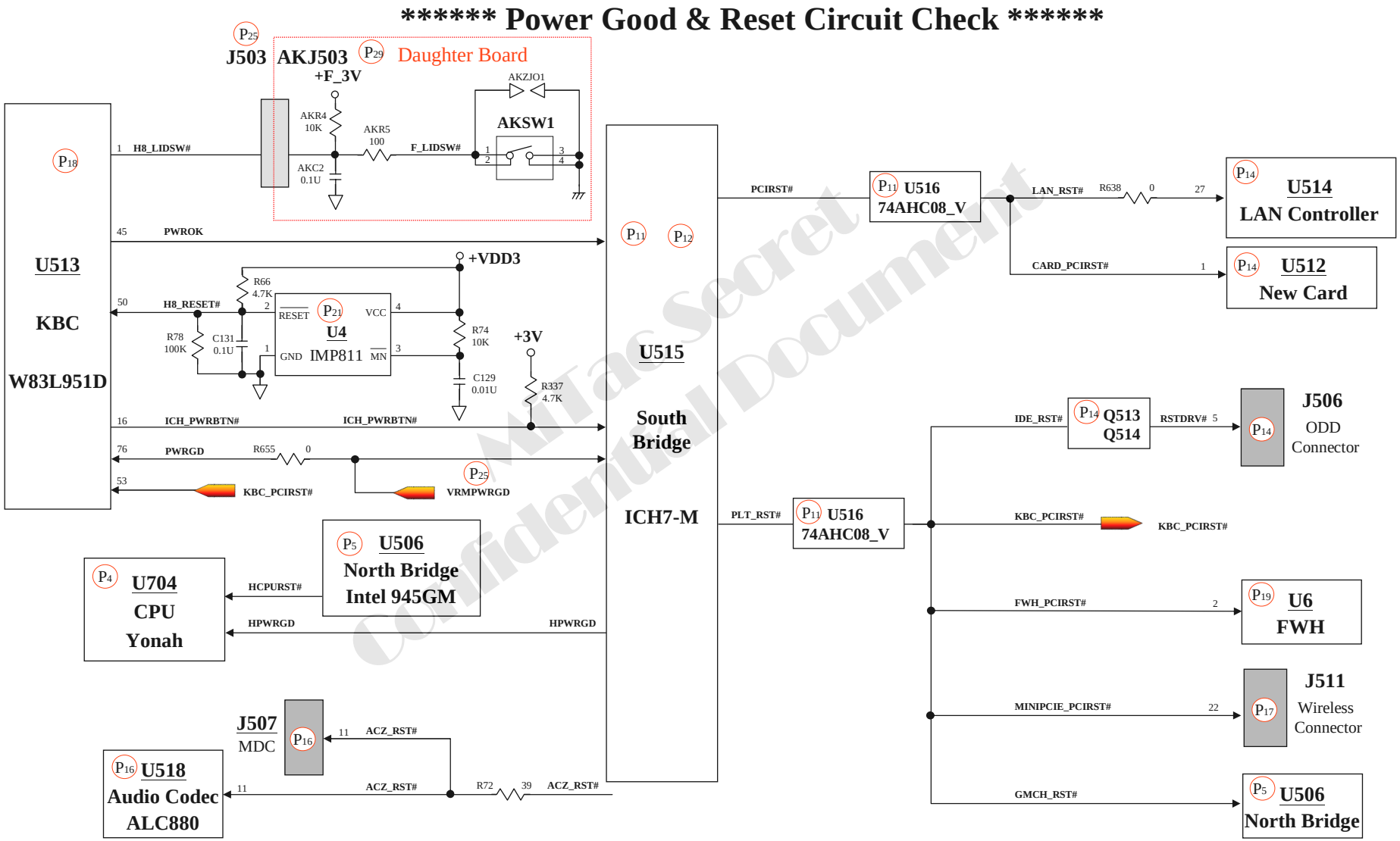
8.2 No Display-3



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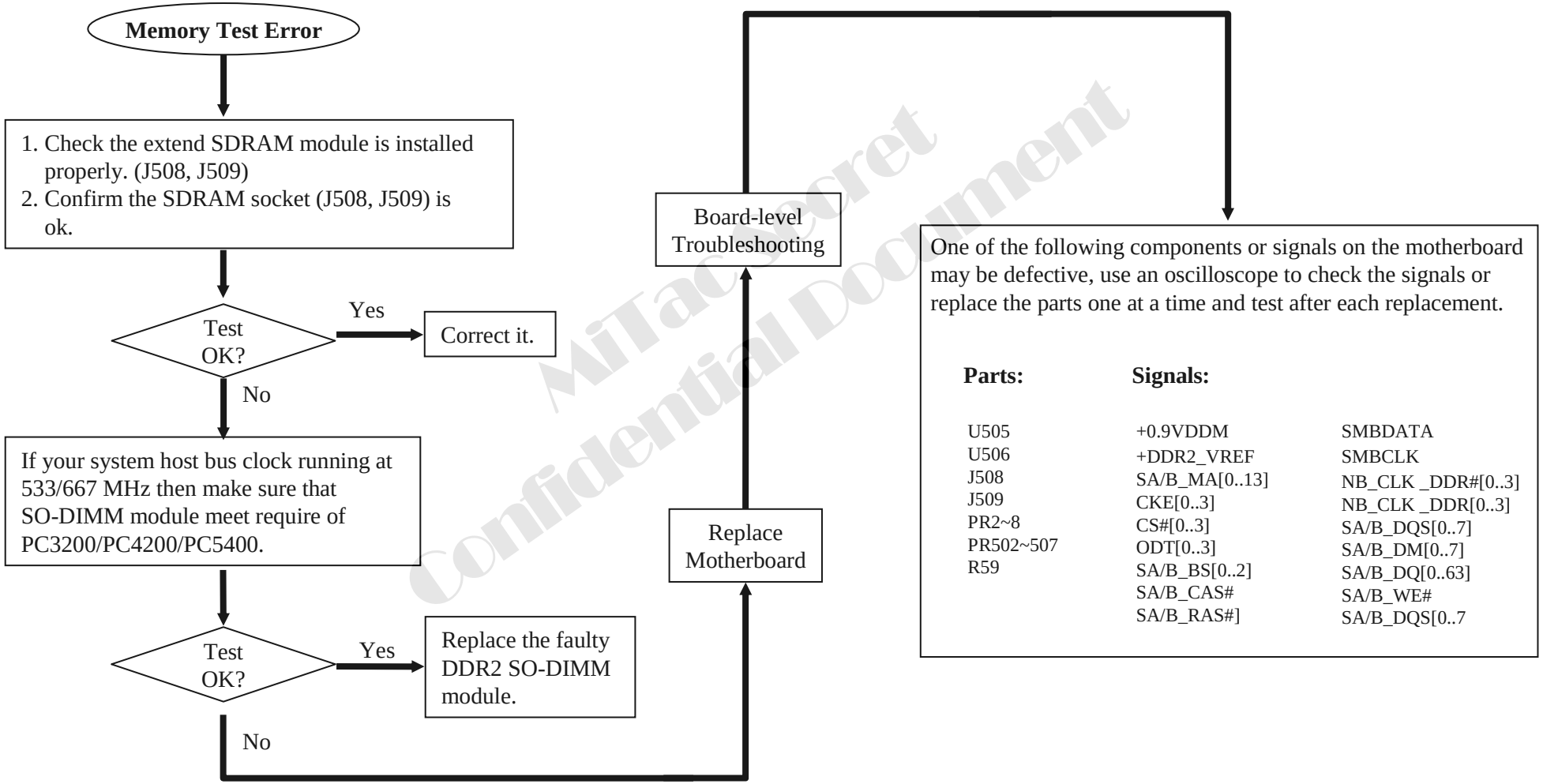
8.3 Memory Test Error-1

Extend DDR2 SO-DIMM is test error or system hangs up.



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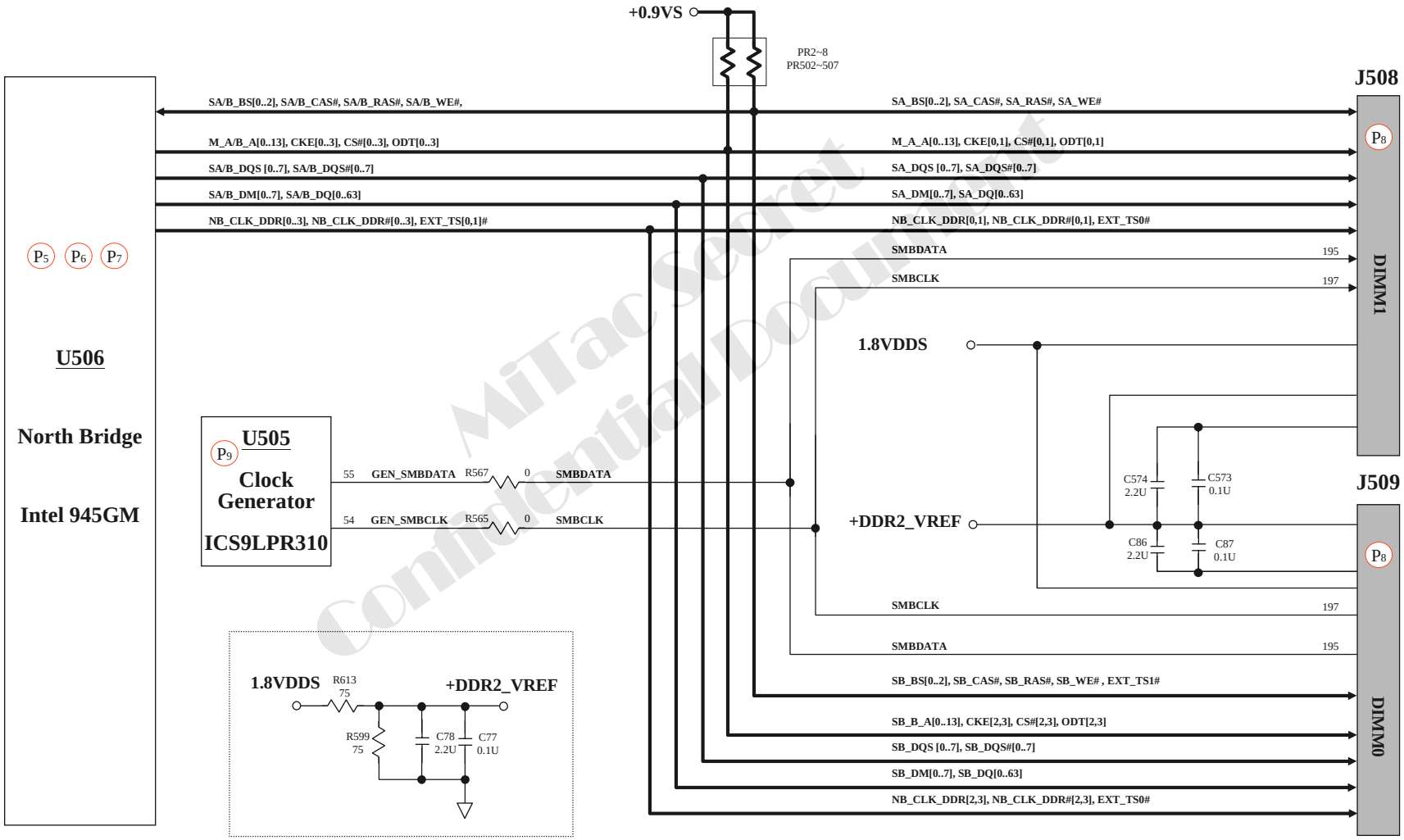
8.3 Memory Test Error-2

Extend DDR2 SO-DIMM is test error or system hangs up.



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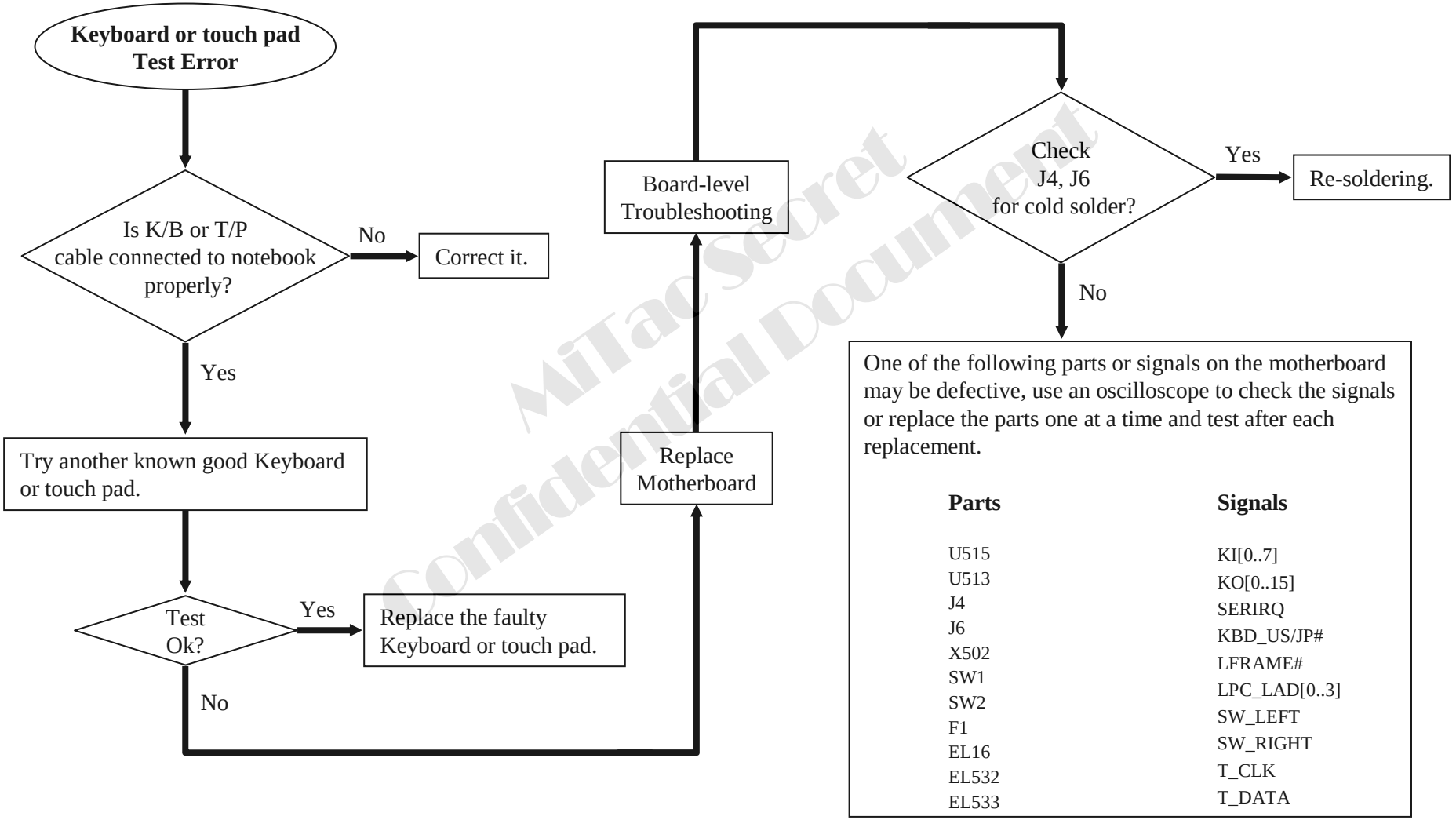
8.4 Keyboard (K/B) or touch pad (T/P) Test Error-1

Error message of keyboard or touch pad test error is shown or any key does not work.



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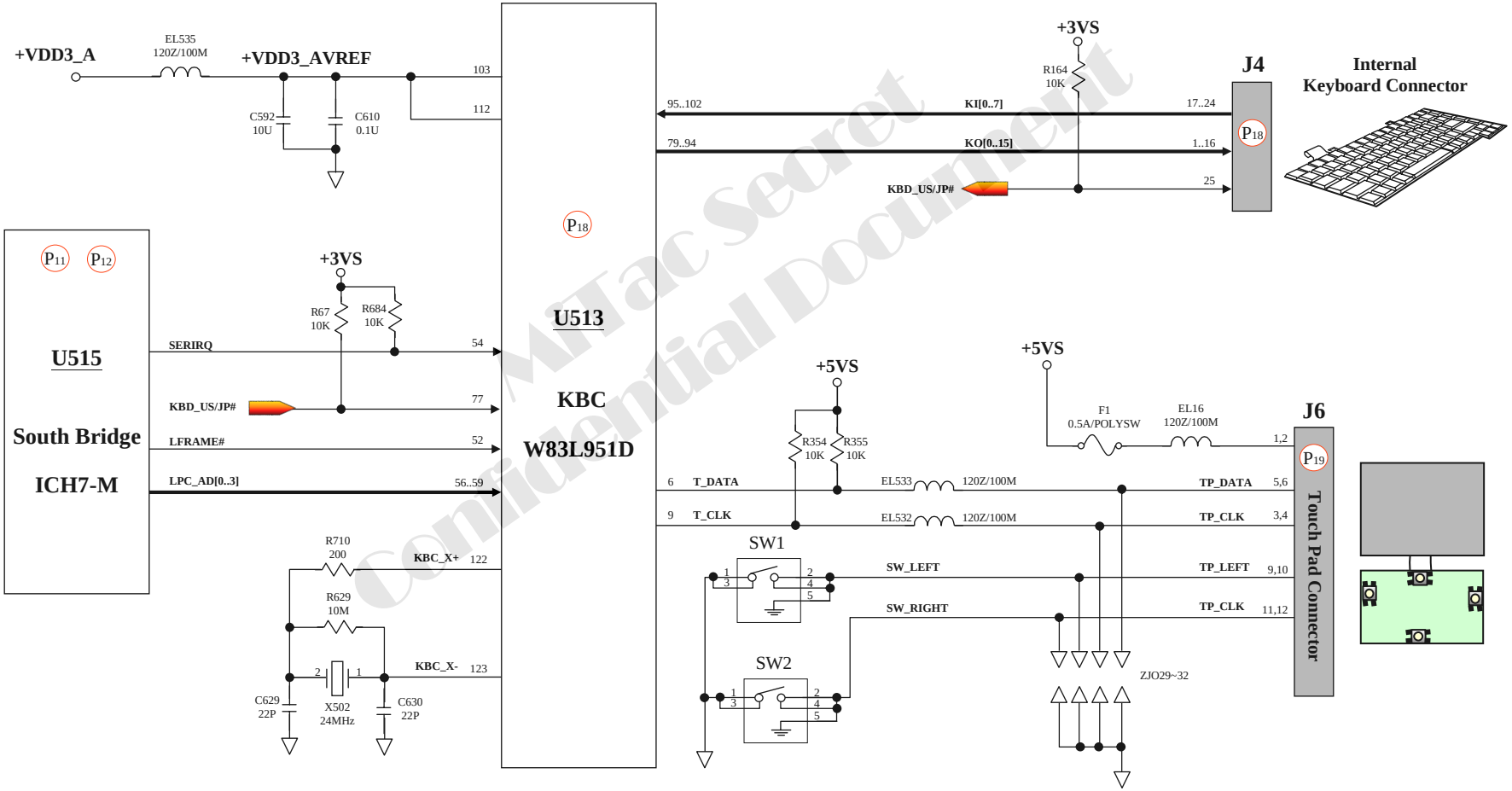
8.4 Keyboard (K/B) or touch pad (T/P) Test Error-2

Error message of keyboard or touch pad test error is shown or any key does not work.



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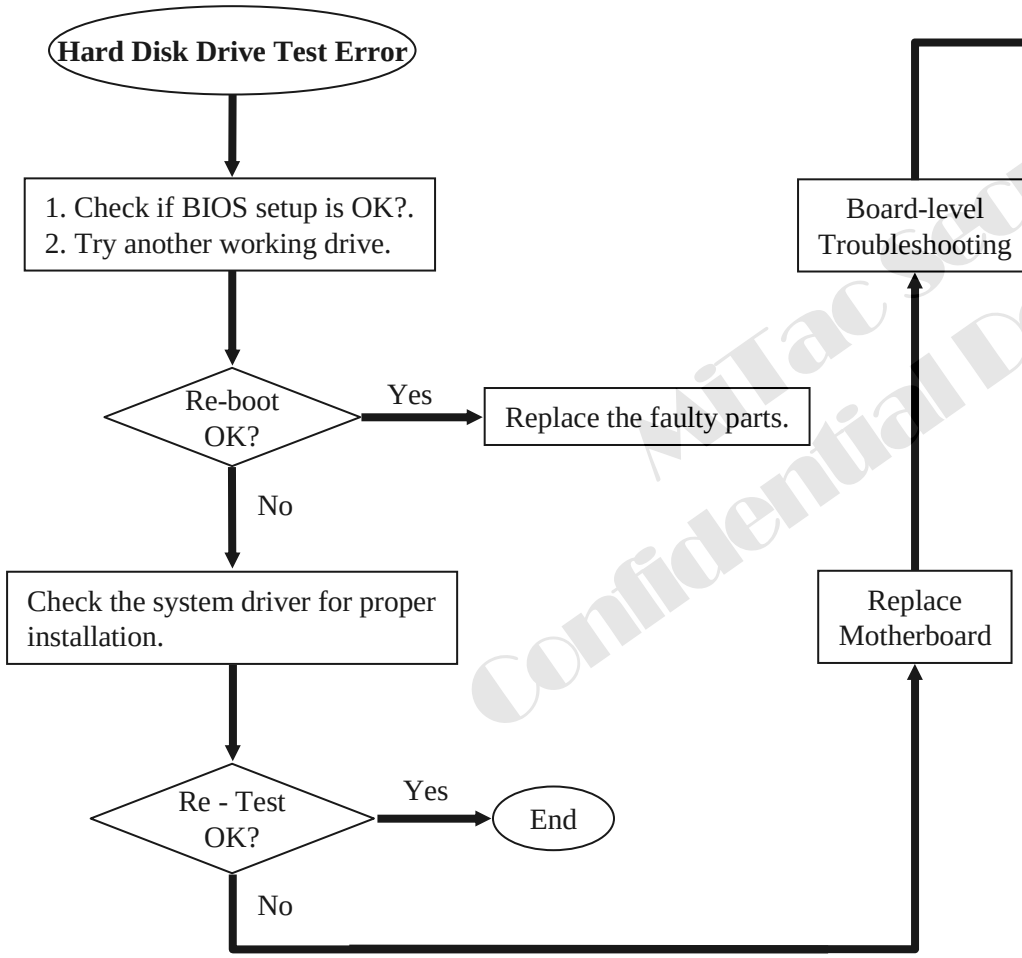
8.5 Hard Disk Drive Test Error-1

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U515	+5VS
J510	+3VS
EL537	+5VS_HDD
D7	SATA_RXP0
D8	SATA_RXN0
C611	SATA_TXP0
C631	SATA_TXN0
C642~645	HDD_LED#
	SATA_LED#

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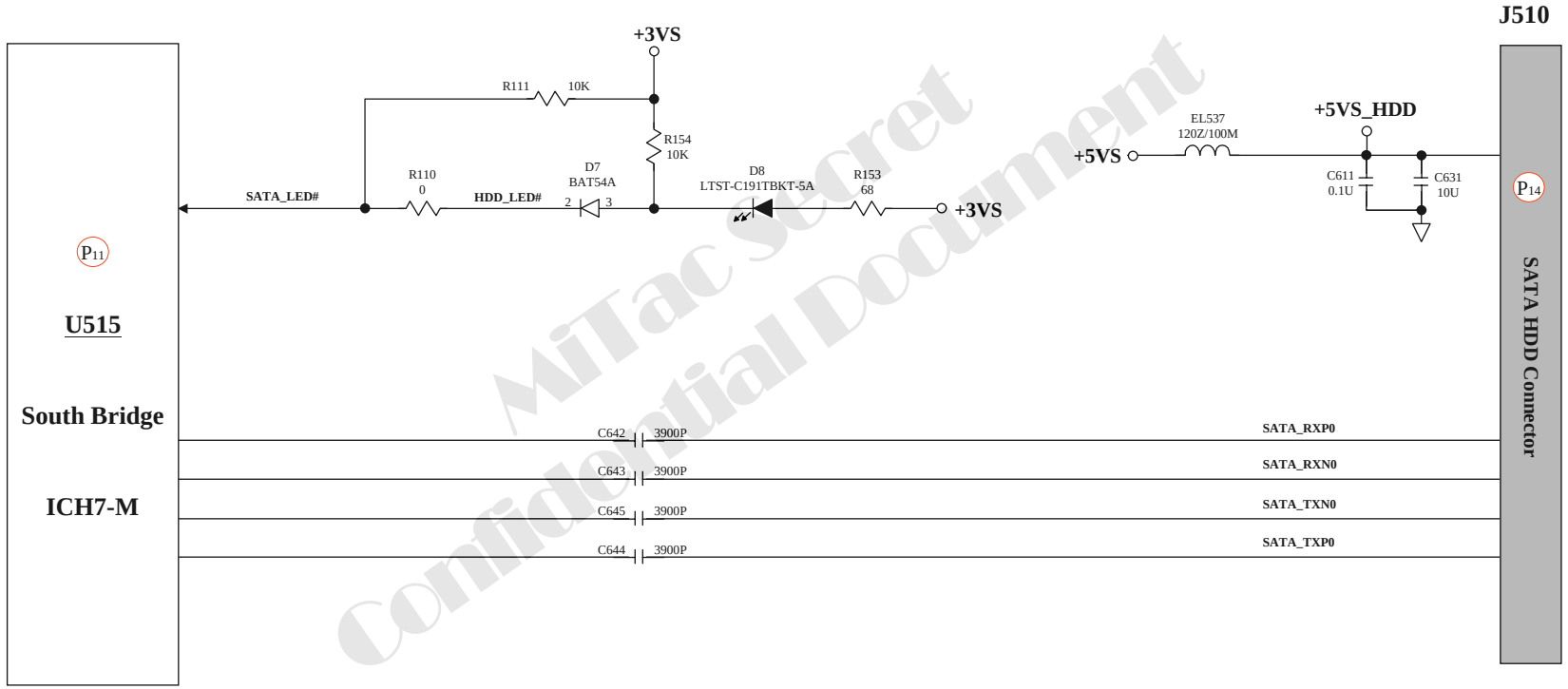
8.5 Hard Disk Drive Test Error-2

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



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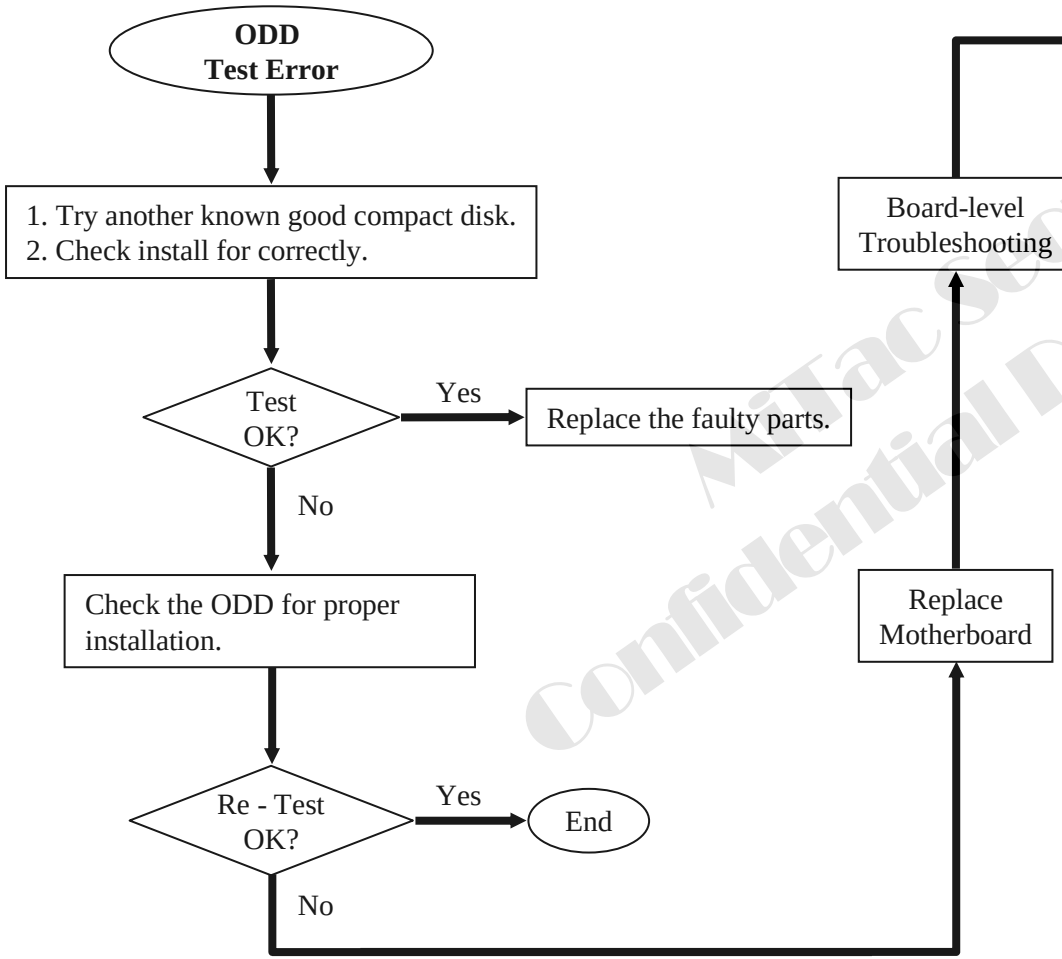
8.6 ODD Test Error-1

An error message is shown when reading data from ODD.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U515	+5VS
U518	+3VS
J506	ODD_LED#
EL18	IDE_RST#
L31	SD_DD[0..15]
Q513	SDCS[1,3]#
Q514	SDA[0..2]
D7	SDDACK
D8	SDIOR#
R119~124	SDIOW#
R617~618	SDDREQ
R153~514	RSTDRV#

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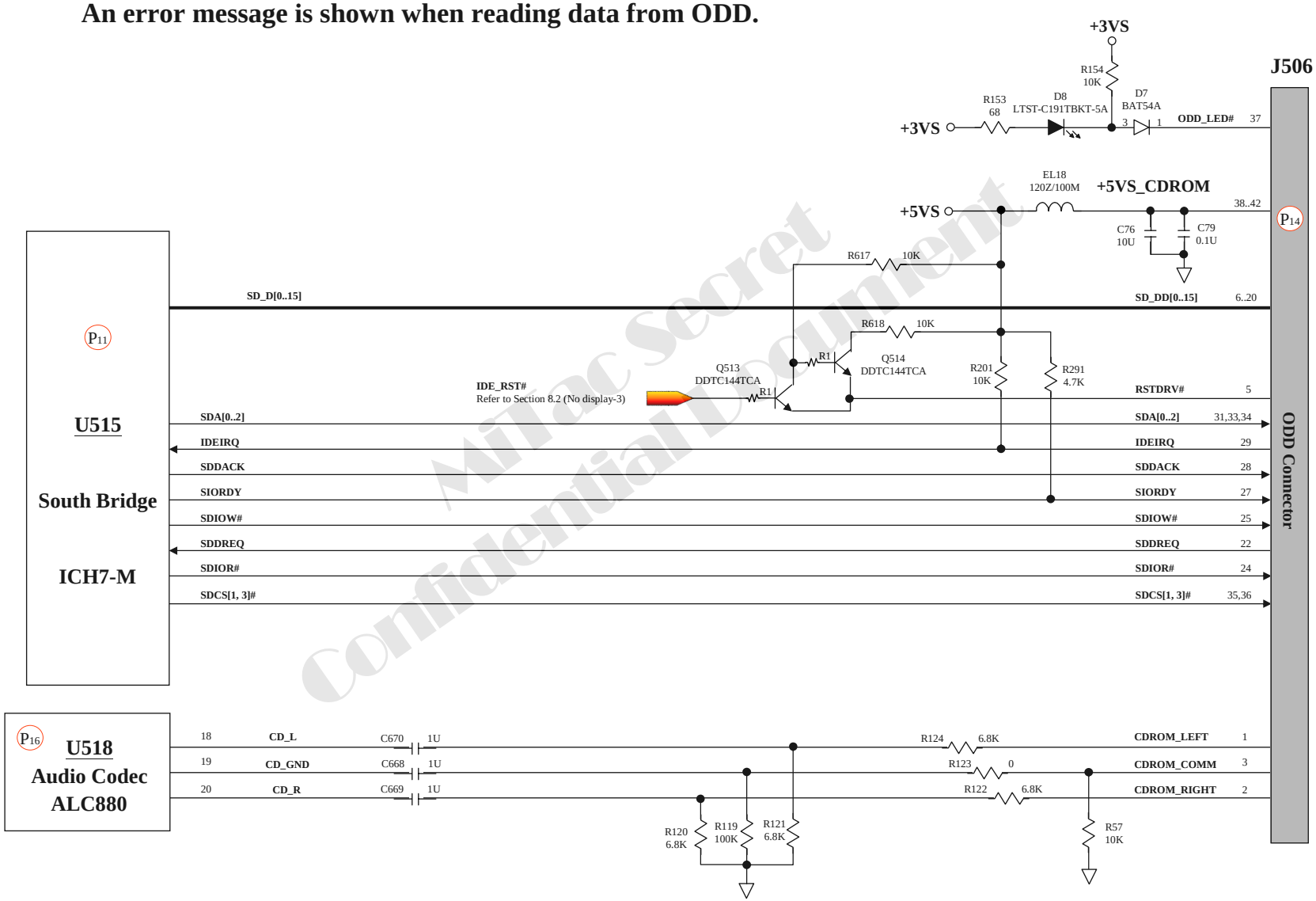
8.6 ODD Test Error-2

An error message is shown when reading data from ODD.



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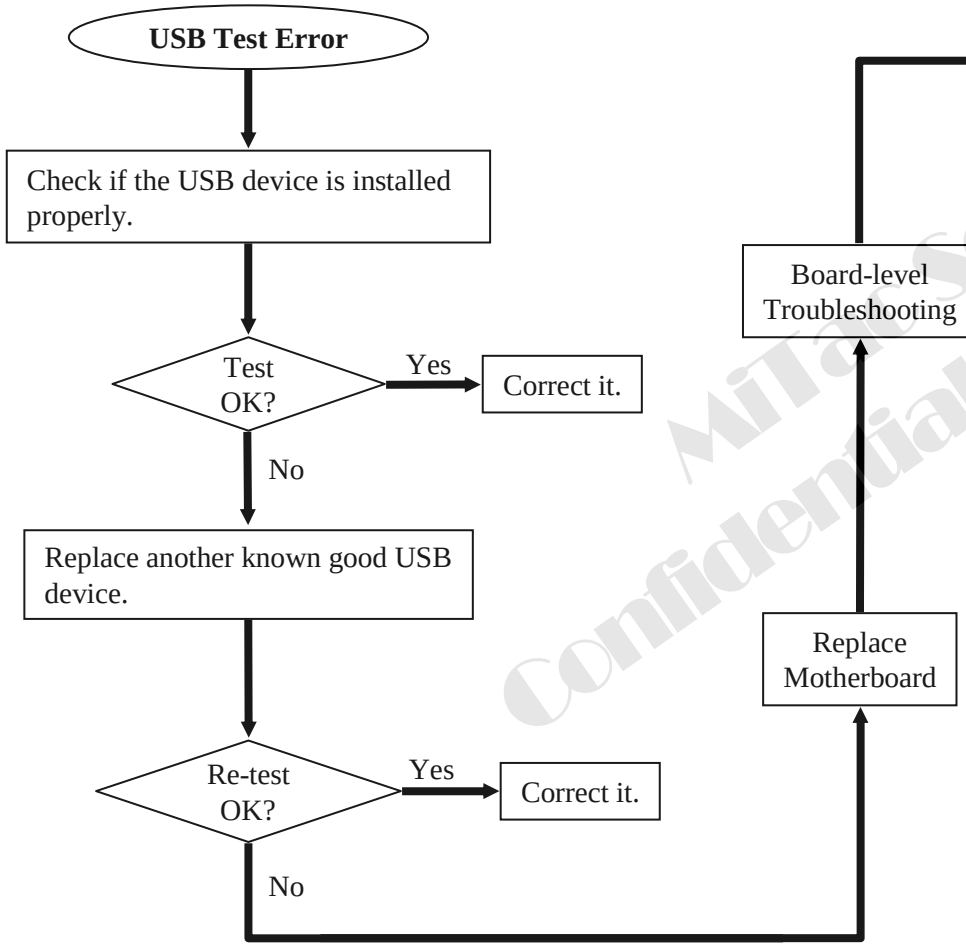
8.7 USB Test Error-1

An error occurs when a USB I/O device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U515	+F5V
AKU501	+F3V
AKU502	SUSC#
AKJ502	F_SUSC#
AKJ504	USB_OC01#
AKEL1~2	F_USB_OC01#
AKEL503~504	USB_OC23#
AKEL501~502	F_USB_OC23#
AKEL505~506	D/USBP[0..3]+
D13	D/USBP[0..3]-
AKR503	F_USBP[0..3]+
AKR505	F_USBP[0..3]-

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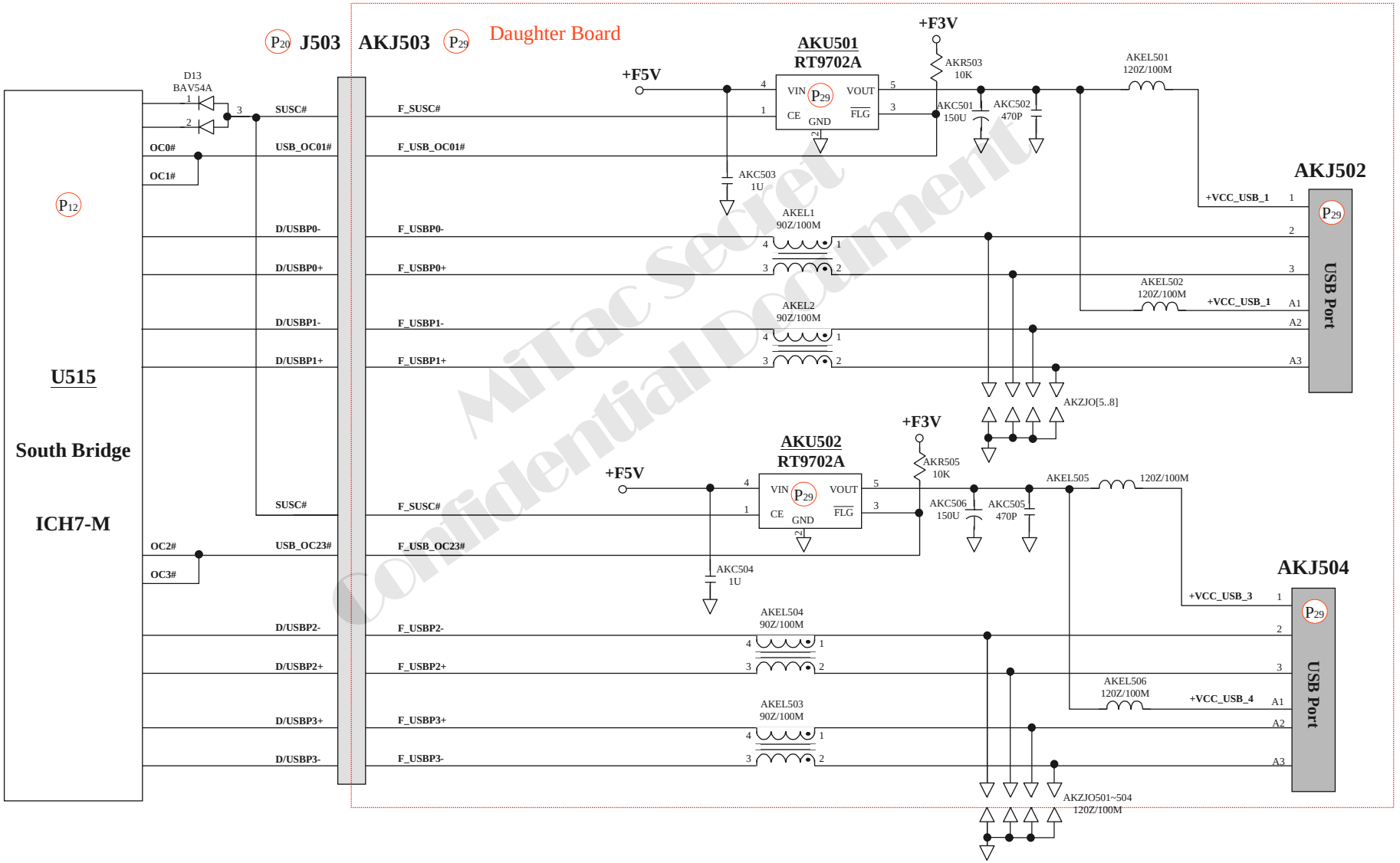
8.7 USB Test Error-2

An error occurs when a USB I/O device is installed.



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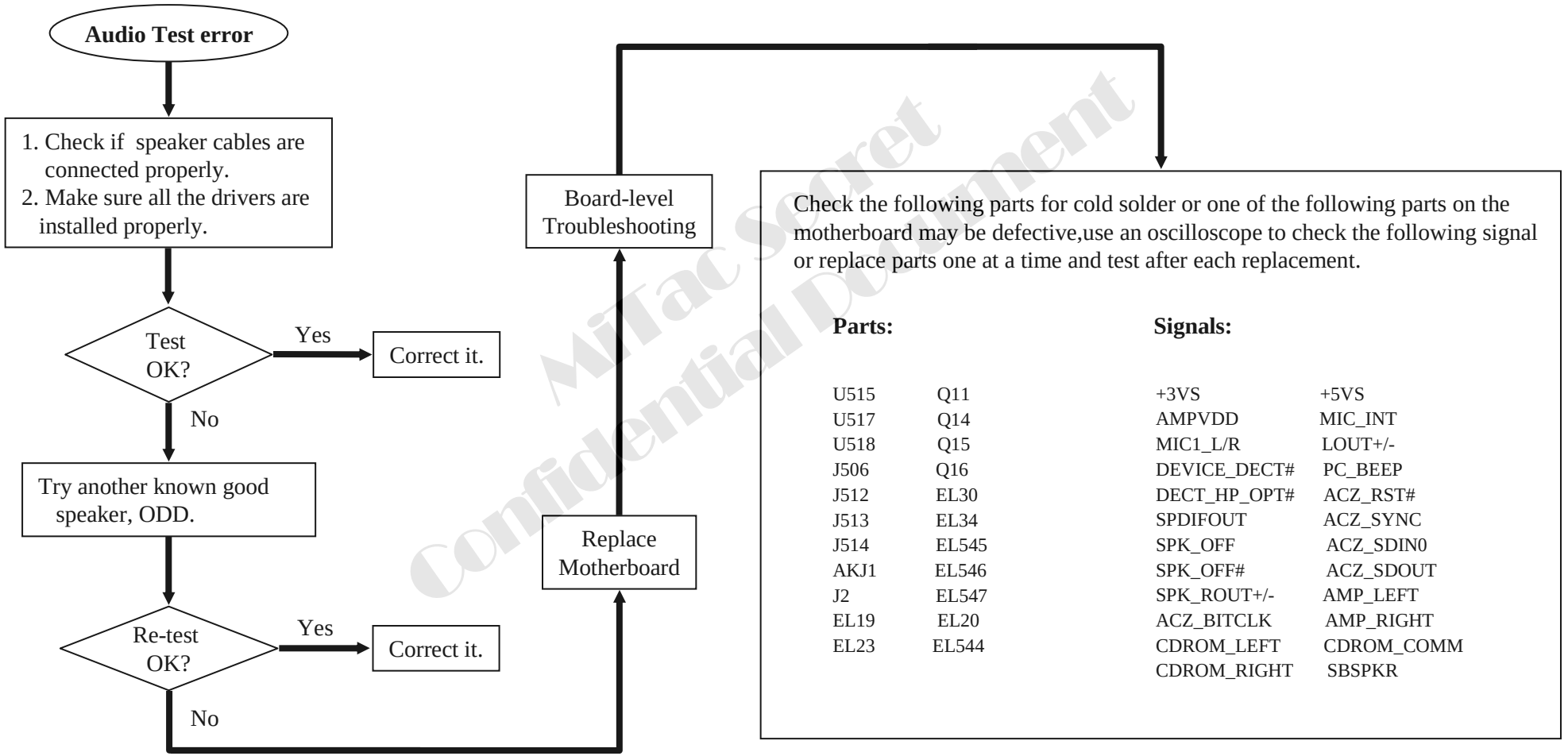
8.8 Audio Test Error-1

No sound from speaker after audio driver is installed.



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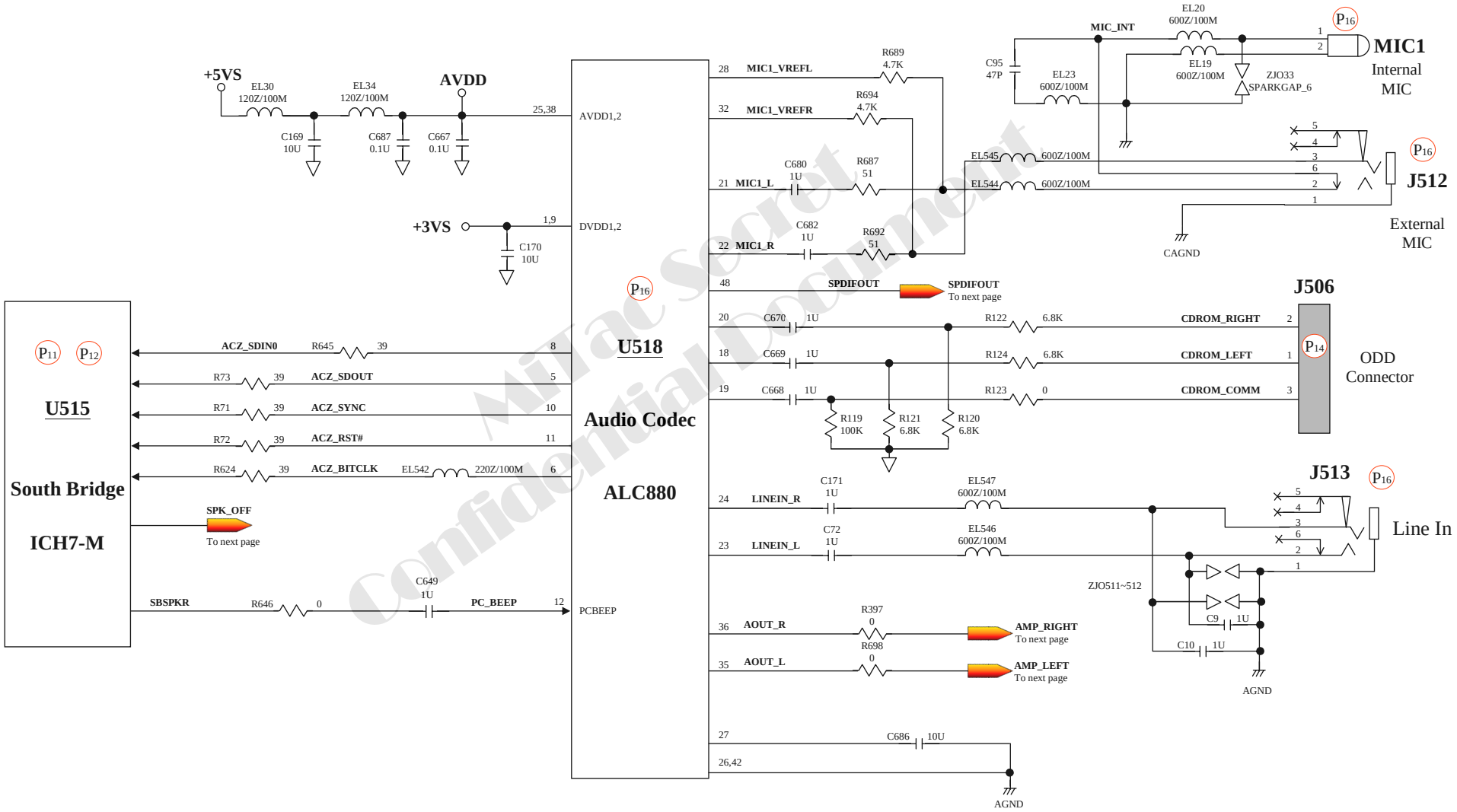
8.8 Audio Test Error-2 (Audio In)

No sound from speaker after audio driver is installed.



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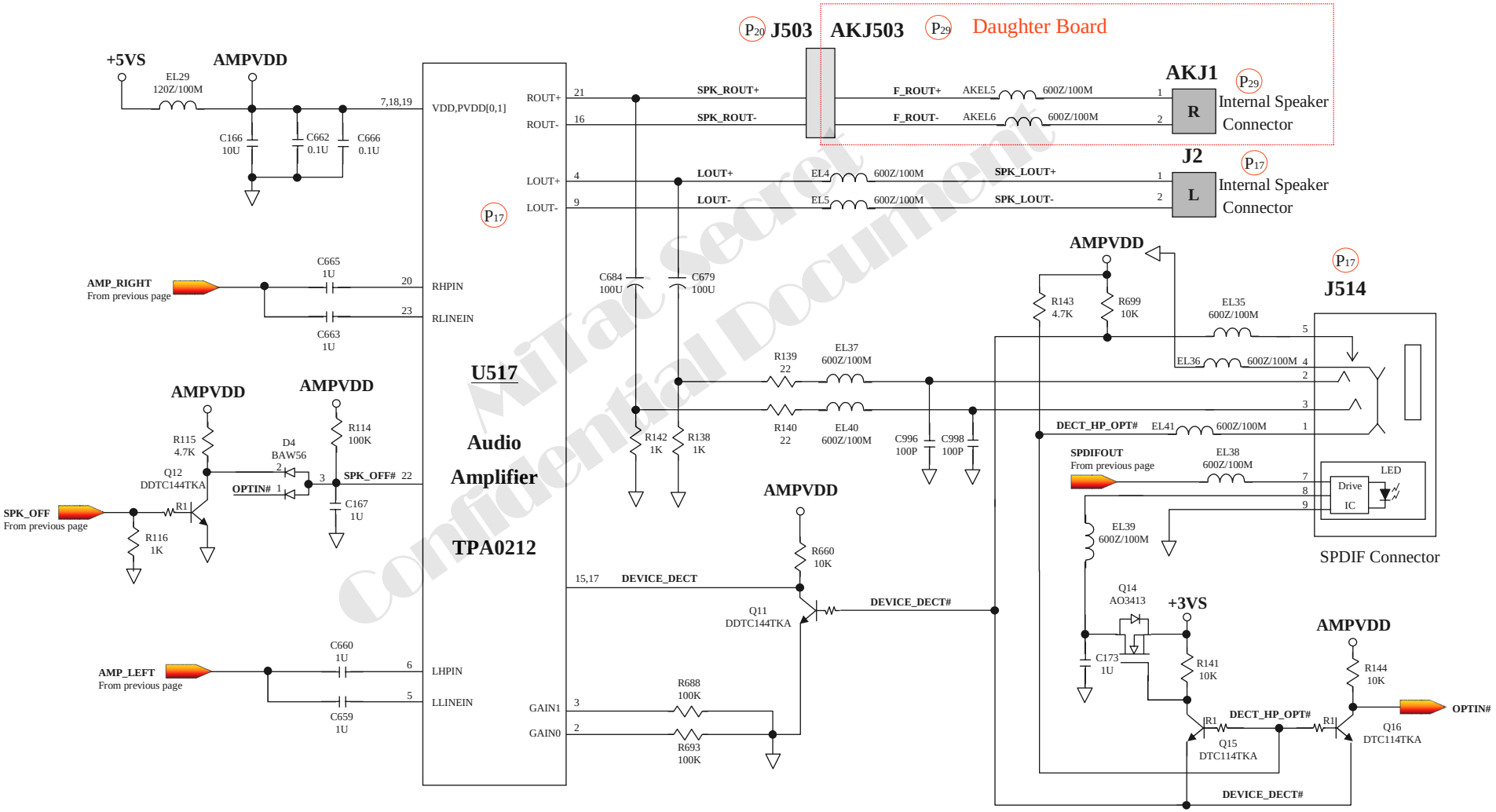
8.8 Audio Test Error-3 (Audio Out)

No sound from speaker after audio driver is installed.



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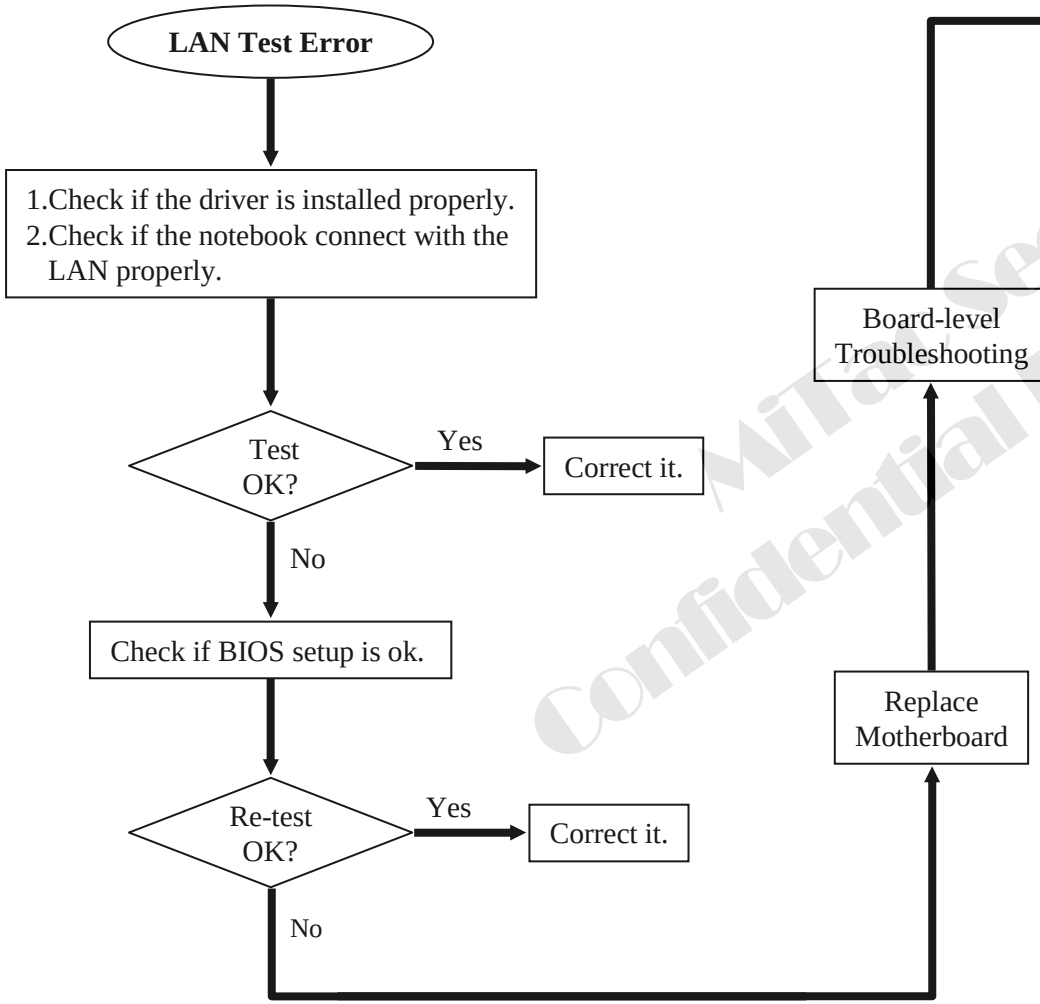
8.9 LAN Test Error-1

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**	
U515	+3V	+2.5V
U514	DVDD	AVDDL
U510	MDI[0,1]+/-	TX+/-
J505	WAKE_UP#	MCT3/4
X503	LAN_RST#	PJ7/4
Q525	PCICLK_LAN	RX+/-
EL530	LAN_WAKE	PJTX+/-
EL531	PCI_AD[0..31]	PJRX+/-
EL541	PCI_C/BE#[0..3]	PCLK_RUN#
EL543	PCI_INTE#	PCI_STOP#
EL540	PCI_IRDY#	PCI_TRDY#
R606~609	PCI_PAR	PCI_PERR#
R631~639	PCI_PME#	PCI_GNT0#
R651	PCI_REQ0#	PCI_FRAME#
R653	PCI_DEVSEL#	

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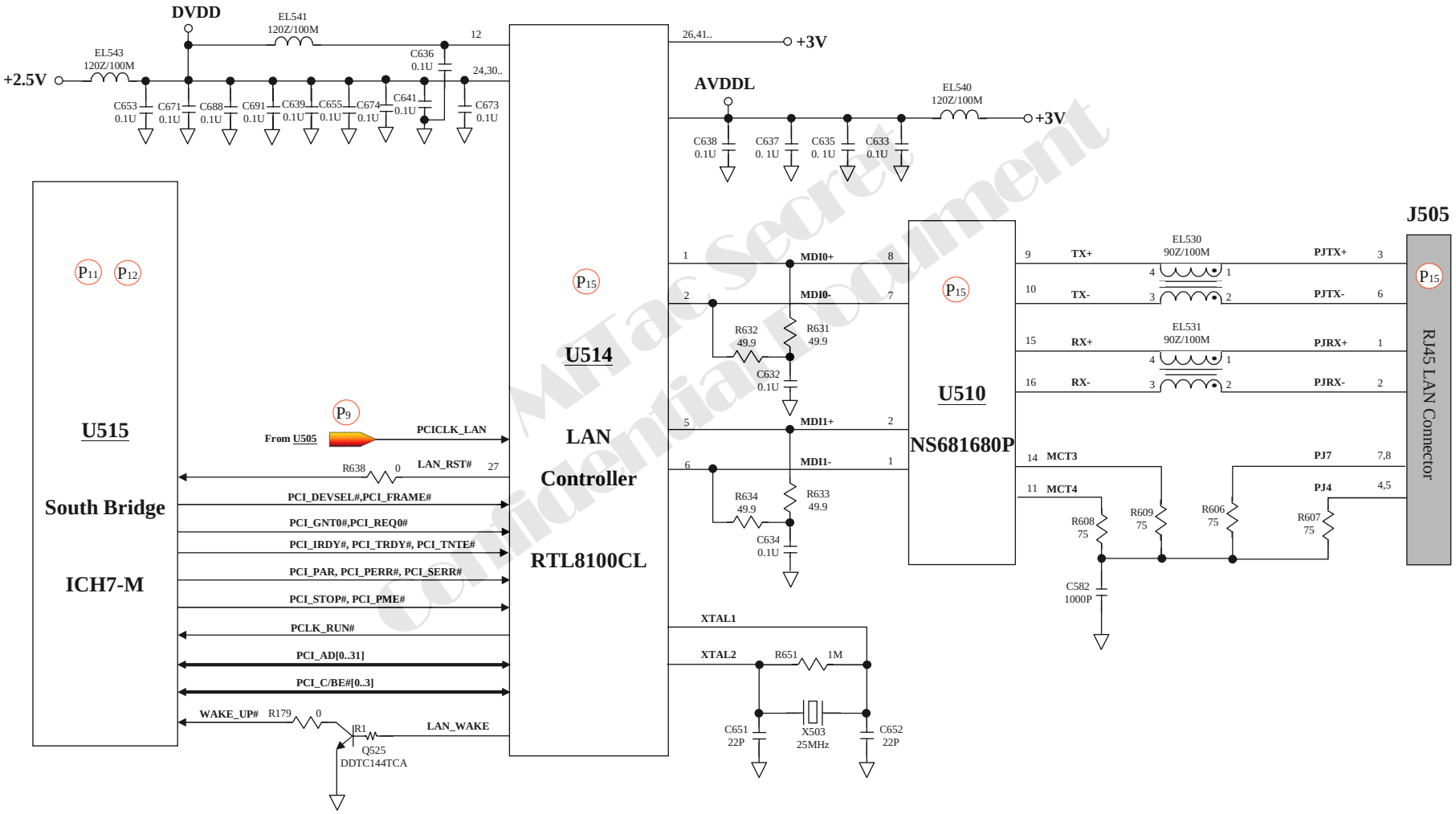
8.9 LAN Test Error-2

An error occurs when a LAN device is installed.



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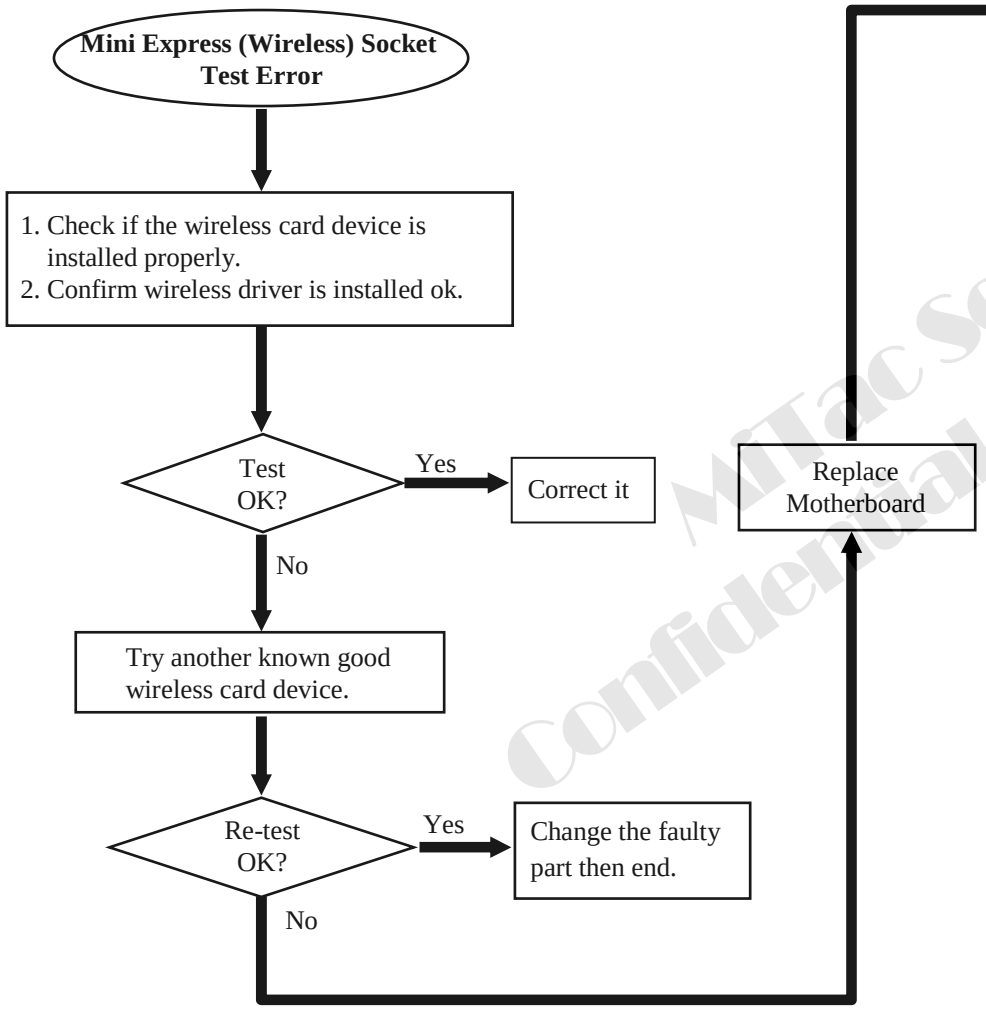
8.10 Mini Express (Wireless) Socket Test Error-1

An error occurs when a wireless card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals	
U505	+3VS	SIO_48M
U515	PCIE_PERN1	SMBCLK
J511	PCIE_PERP1	SMBDATA
R661	PCIE_PETN1	USBPCIEP6-/+
R659	PCIE_PETP1	MINIPCIE_PCIRST#
C191	LAD[0..3]	WIRELESS_PD#
C192	LFRAME#	
R134	LDRQ0#	
R689	MINIPCIE_CLKREQ1#	
PR510	MINIPCIECLK1#	
PR508	MINIPCIECLK1	

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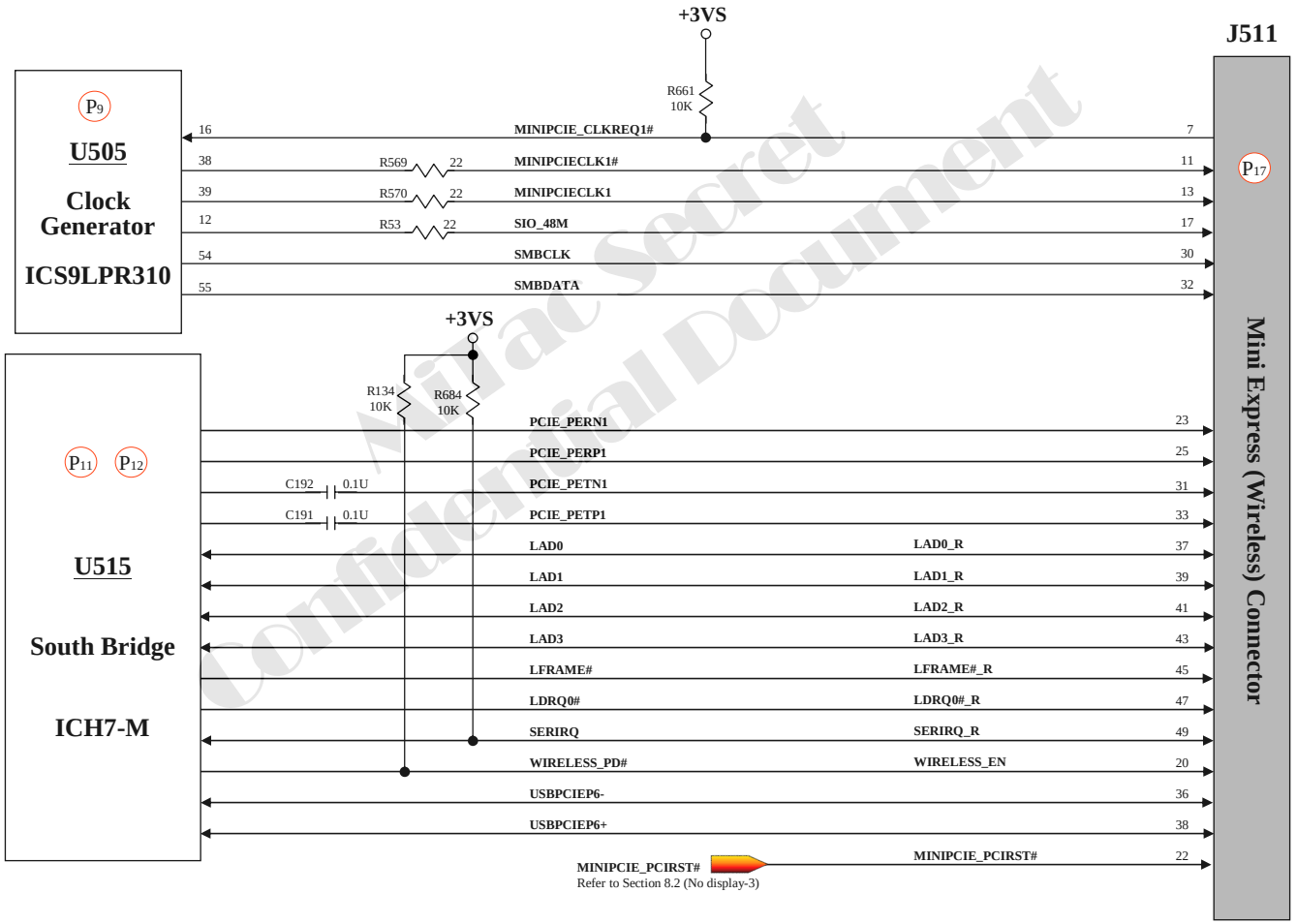
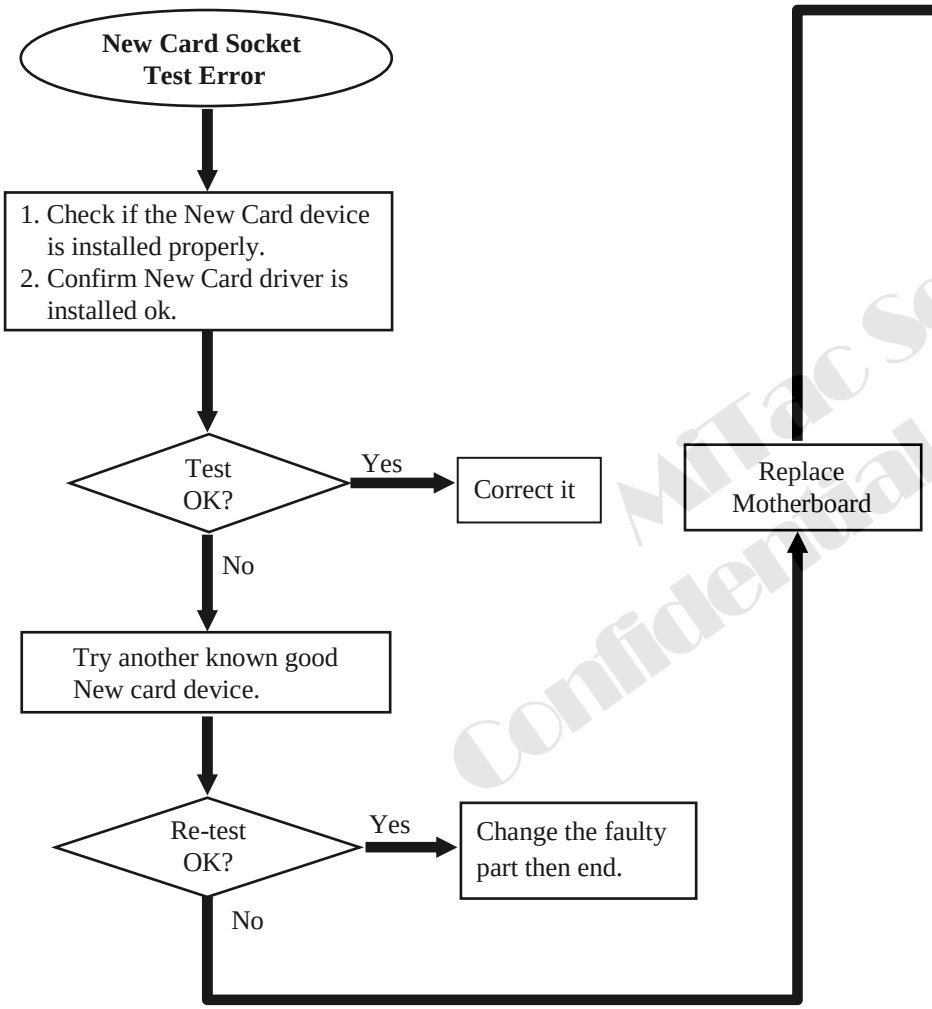
8.10 Mini Express (Wireless) Socket Test Error-2

An error occurs when a wireless card device is installed.



8.11 New Card Socket Test Error-1

An error occurs when a express card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U505	+3V	NEWCARD_PERN0
U515	+3VS	NEWCARD_PERP0
U512	+1.5VS	NEWCARD_PETN0
J8	CARD_+3.3VS	NEWCARD_PETP0
Q524	CARD_3.3V	CPPE#
R50	CARD_+1.5VS	PREST#
RP509	PCIECLK_NCARD	SMBCLK
C189	PCIECLK_NCARD#	SMBDATA
C190	PCI_PME#	

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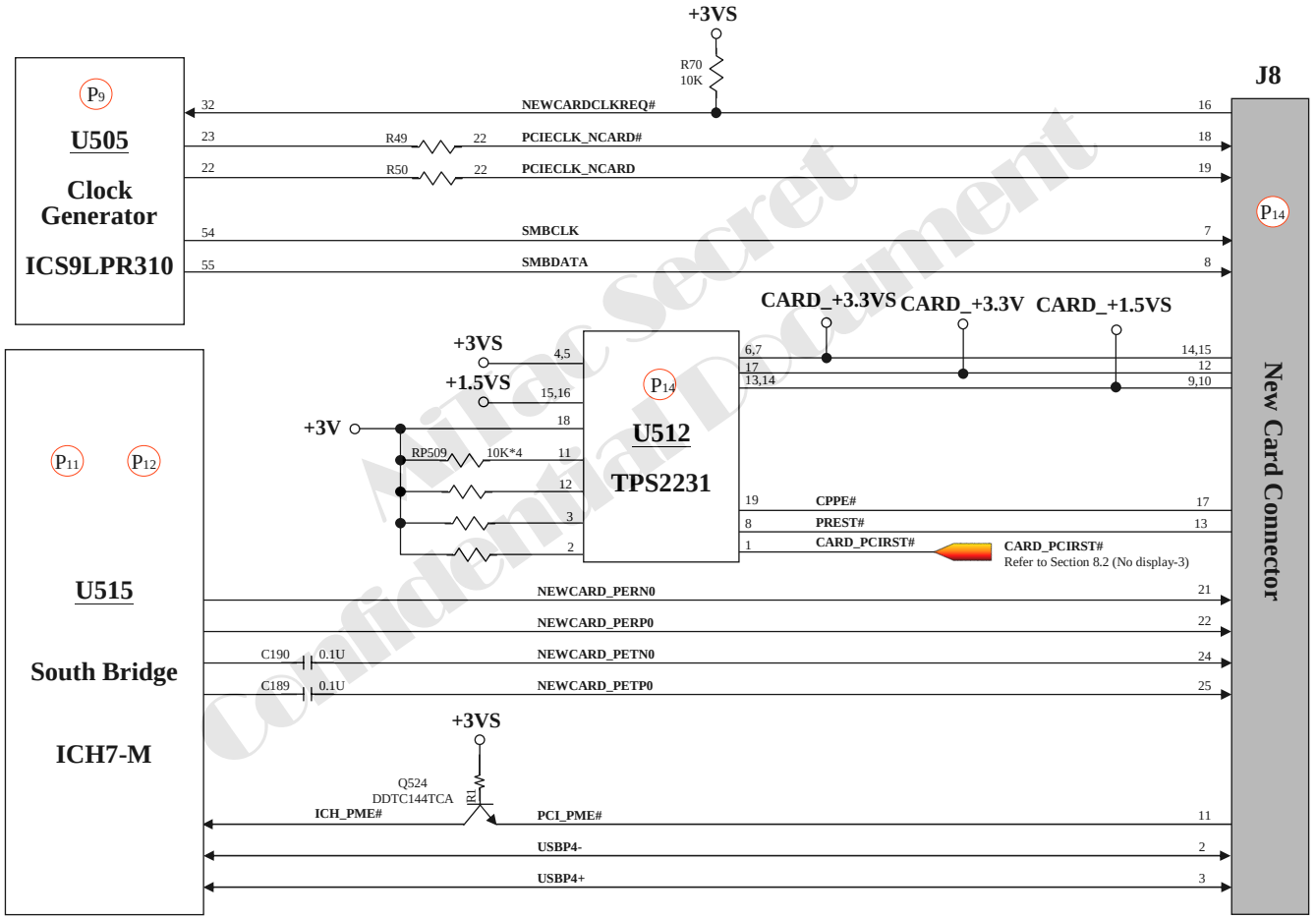
8.11 New Card Socket Test Error-2

An error occurs when a express card device is installed.



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9. Spare Parts List --1

Part Number	Description	Location(s)
526280732003	LTSPMAX;8258IID3/G5A2/0I10I/3XES	
416280732002	CFM-MEDION-LT PF;15.4",WXGA,LG,G	
442600000077	TF041-TOUCHPAD MODULE;TM61PDM1G2	
411807320001	TF041-PWA;PWA-8258I-MAX,MOTHER B	
411807320003	TF041-PWA;PWA-8258I-MAX,MOTHER B	
271002000312	TF041-TH-RES;0 ,1/10W,5% ,080	EL31
271002102312	TF041-TH-RES;1K ,1/10W,5% ,080	R41,R614
271002221304	TF041-TH-RES;220,1/8W,5%,0805,SM	PR520,PR524
271002472304	TF041-TH-RES;4.7K ,1/10W,5% ,080	PR22,PR23
271061000003	TF041-TH-RES;0 ,1/16W,0402,SM	PR18,PR26,PR27,PR29,PR30
271061100103	TF041-TH-RES;10,1/16W,1%,0402,SM	PR39,PR40,PR45,PR48,PR510
271061100312	TF041-TH-RES;10 ,1/16W,5% ,040	PR74
271061101109	TF041-TH-RES;100 ,1/16W,1% ,040	R37,R47,R550,R556,R652
271061102113	TF041-TH-RES;1K ,1/16W,1% ,040	PR566,PR567,R116,R129,R138,R1
271061102310	TF041-TH-RES;1K ,1/16W,5% ,040	R635
271061103114	TF041-TH-RES;10K ,1/16W,1% ,040	PR46,PR512,PR516,PR534,PR536
271061103307	TF041-TH-RES;10K ,1/16W,5% ,040	PR505,R154,R617,R618
271061104108	TF041-TH-RES;100K ,1/16W,1% ,040	PR13,PR20,PR514,PR546,R114,R
271061104306	TF041-TH-RES;100K ,1/16W,5% ,040	PR521,PR532
271061105307	TF041-TH-RES;1M ,1/16W,5% ,040	PR525,PR533,PR553,PR554,R100
271061106308	TF041-TH-RES;10M ,1/16W,5% ,040	R102,R629
271061151110	TF041-TH-RES;150 ,1/16W, 1%,040	R1,R2,R21,R22,R23,R3,R536,R537
271061153110	TF041-TH-RES;15K ,1/16W,1% ,040	R636
271061201107	TF041-TH-RES;200 ,1/16W, 1%,040	R36,R710
271061202104	TF041-TH-RES;2K ,1/16W,1% ,040	R520

Part Number	Description	Location(s)
271061203112	TF041-TH-RES;20K ,1/16W,1% ,040	PR501
271061220308	TF041-TH-RES;22 ,1/16W,5% ,040	R139,R140,R49,R50,R51,R53,R56
271061222104	TF041-TH-RES;2.2K,1/16W,1%,0402,	R126,R52,R573,R575,R675
271061240102	TF041-TH-RES;24.9,1/16W,1% ,0402	R168,R28,R554,R582,R654,R723
271061270104	TF041-TH-RES;27.4 ,1/16W, 1%,04	R14,R522,R583,R584
271061272105	TF041-TH-RES;2.7K ,1/16W,1% ,040	R81,R82
271061330311	TF041-TH-RES;33 ,1/16W,5% ,040	R517,R56,R574,R580,R593,R594,I
271061390309	TF041-TH-RES;39, 1/16W, 5%,0402	R19,R20,R39,R40,R503,R504,R61
271061471308	TF041-TH-RES;470 ,1/16W,5% ,040	PR550,PR551,R598
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,040	R101,R125,R143,R26,R501,R505,I
271061490102	TF041-TH-RES;49.9 ,1/16W,1% ,040	R631,R632,R633,R634
271061492102	TF041-TH-RES;4.99K,1/16W,1% ,040	PR79,R35
271061494101	TF041-TH-RES;499K ,1/16W,1% ,04	PR19
271061510306	TF041-TH-RES;51, 1/16W, 5%,0402	R524,R687,R692
271061540102	TF041-TH-RES;54.9 ,1/16W,1% ,040	R10,R11,R12,R13,R523,R551,R55
271061560306	TF041-TH-RES;56 ,1/16W,5% ,040	R15,R526,R707,R724
271061562107	TF041-TH-RES;5.6K ,1/16W, 1%,04	R650
271061680305	TF041-TH-RES;68,1/16W,5%,0402,SM	R145,R150,R153,R158,R159,R162
271061682304	TF041-TH-RES;6.8K ,1/16W,5% ,04	R120,R121,R122,R124
271061750105	TF041-TH-RES;75,1/16W,1%,0402,SM	R599,R606,R607,R608,R609,R613
271061822307	TF041-TH-RES;8.2K ,1/16W,5% ,040	R107,R127,R164,R558,R603,R667
271071000312	TF041-TH-RES;0 ,1/16W,5% ,060	EL25,EL27,PR25,PR506,PR70
271071010304	TF041-TH-RES;1 ,1/16W,5% ,060	R169,R45
271071100103	TF041-TH-RES;10 ,1/16W,1% ,060	PR552,PR558
271071102107	TF041-TH-RES;1K ,1/16W,1% ,060	PR34,PR526

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Part Number	Description	Location(s)
271071103108	TF041-TH-RES;10K ,1/16W,1% ,060	PR14,PR564
271071104108	TF041-TH-RES;100K ,1/16W,1% ,060	PR563
271071112106	TF041-TH-RES;1.13K,1/16W,1%,0603	PR529
271071113115	TF041-TH-RES;11.8K ,1/16W,1% ,06	PR38
271071122105	TF041-TH-RES;1.2K ,1/16W,1% ,060	PR49,PR540,PR556
271071124117	TF041-TH-RES;124K ,1/16W,1% ,060	PR10
271071133114	TF041-TH-RES;13.7K,1/16W,.1%,060	PR15
271071152107	TF041-TH-RES;1.5K ,1/16W,1% ,060	R533
271071154115	TF041-TH-RES;150K ,1/16W,1% ,060	PR69
271071181103	TF041-TH-RES;180 ,1/16W,1% ,060	PR53
271071182216	TF041-TH-RES;18.2K,1/16W,1%,0603	PR560
271071184103	TF041-TH-RES;180K ,1/16W,1% ,060	R669
271071203106	TF041-TH-RES;20K ,1/16W,1% ,060	R97
271071203107	TF041-TH-RES;20K ,1/16W,.1%,060	PR28
271071213104	TF041-TH-RES;21.5K,1/16W,1% ,060	PR507,PR518
271071220106	TF041-TH-RES;22.6,1/16W,1%,0603,	R619,R622,R85,R90
271071221103	TF041-TH-RES;221 ,1/16W,1% ,060	R552,R553
271071224102	TF041-TH-RES;226K ,1/16W,1% ,060	PR21
271071228306	TF041-TH-RES;2.2 ,1/16W,5% ,060	PR508,PR519,PR522,PR523,PR54
271071237212	TF041-TH-RES;23.7K,1/16W,1% ,060	PR17
271071242104	TF041-TH-RES;2.49K,1/16W,1% ,060	PR12
271071251101	TF041-TH-RES;255 ,1/16W,1% ,0603	R34
271071292101	TF041-TH-RES;2.94K ,1/16W,1% ,06	PR31
271071304104	TF041-TH-RES;300K ,1/16W,1% ,060	PR544
271071332313	TF041-TH-RES;332K ,1/16W,1% ,060	R98

Part Number	Description	Location(s)
271071362102	TF041-TH-RES;3.6K ,1/16W,1% ,060	R665
271071394305	TF041-TH-RES;390K ,1/16W,5% ,060	PR543
271071432113	TF041-TH-RES;4.3K ,1/16W,1% ,060	PR51
271071452101	TF041-TH-RES;4.53K ,1/16W,1% ,06	PR33
271071472309	TF041-TH-RES;4.7K ,1/16W,5% ,060	PR41,PR42
271071473103	TF041-TH-RES;47K ,1/16W,1% ,060	PR569
271071478304	TF041-TH-RES;4.7 ,1/16W,5% ,060	PR71
271071512103	TF041-TH-RES;5.1K ,1/16W,1% ,060	PR509,PR68
271071612101	TF041-TH-RES;6.19K,1/16W,1% ,060	PR9
271071642101	TF041-TH-RES;6.49K,1/16W,1% ,060	PR537
271071682103	TF041-TH-RES;6.8K ,1/16W,1% ,060	PR52
271071683102	TF041-TH-RES;68K ,1/16W,1% ,060	PR538
271071683103	TF041-TH-RES;68.1K ,1/16W,1% ,06	PR50
271071752105	TF041-TH-RES;7.5K,1/16W,1%,0603,	PR24
271071753102	TF041-TH-RES;75K ,1/16W,1% ,060	PR568
271071800101	TF041-TH-RES;80.6 ,1/16W,1% ,060	R600,R601
271072263101	TF041-TH-RES;26.7K,1/10W,1% ,060	PR559
271072372101	TF041-TH-RES;37.4K ,1/10W,1% ,06	PR535
271072394102	TF041-TH-RES;392K ,1/10W,1% ,060	PR16
271072482101	TF041-TH-RES;4.87K,1/10W,1%,0603	PR35
271072562101	TF041-TH-RES;56.2K ,1/10W,1% ,06	PR555
271611103305	TF041-TH-RP;10K*4 ,8P ,1/16W,5%	RP11,RP501,RP509,RP514
271611560305	TF041-TH-RP;56*4 ,8P ,1/16W,5%	RP2,RP3,RP4,RP5,RP502,RP503,I
271611822307	TF041-TH-RP;8.2K*4,8P ,1/16W,5%	RP10,RP12,RP15,RP16,RP511,RP
271621103306	TF041-TH-RP;10K*8 ,10P,1/32W,5%	RP14

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Part Number	Description	Location(s)
271621472306	TF041-TH-RP;4.7K*8,10P,1/32W,5%	RP9
272000226501	TF041-TH-CAP;22U ,CR,6.3V,0805,X	C16,C19,C22,C26,C27,C28,C30,C3
272001106514	TF041-TH-CAP;10U,6.3V,+- 20%,080	C115,C123,C124,C125,C130,C166
272002224405	TF041-TH-CAP;0.22U,16V,0805,10%,	PC512,PC527
272002225705	TF041-TH-CAP;2.2U ,CR,16V ,+80-2	C547,C577,C624,C625
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1206	PC504,PC506,PC509,PC514,PC52
272030102411	TF041-TH-CAP;1000P,2KV,10%,1808,	C582,HC3,HC4
272071105411	TF041-TH-CAP;1U ,10V ,10%,0603,X	PC552,PC554,PC570,PC583,PC59
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,10%,	C101,C102,C104,C105,C108,C110
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,0603,	C113,C183,C39,C542,C614,C618,(
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10%,0	PC2
272072153405	TF041-TH-CAP;0.015U ,CR,16V,10%,	PC37
272072224405	TF041-TH-CAP;0.22U ,16V ,10%,060	PC19,PC30,PC43,PC553,PC590
272072473409	TF041-TH-CAP;0.047U,16V ,10%,060	PC582
272073104712	TF041-TH-CAP;0.1U,25V,10%,0603,X	EC7,PC534,PC538,PC543,PC559,
272073105404	TF041-TH-CAP;1UF ,25V,10%,0603,	PC31
272073223408	TF041-TH-CAP;0.022U,CR,25V ,10%,	PC38
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,10%,	C517
272075104710	TF041-TH-CAP;0.1U ,50V,+80-20%,	C4,PC16,PC501,PC507,PC537,PC
272075222704	TF041-TH-CAP;2200P,50V ,+/-20%,0	PC39
272075271408	TF041-TH-CAP;270P ,50V,+-10%,060	PC560,PC563
272075470315	TF041-TH-CAP;47P ,CR,50V ,5%,060	PC561,PC562
272075471415	TF041-TH-CAP;470P ,50V,10%,0603,	PC591
272101016401	TF041-TH-CAP;.1U ,CR,10V,10%,04	PC539
272101105705	TF041-TH-CAP;1U ,CR,6.3V ,80-2	C10,C126,C147,C155,C161,C167,(

Part Number	Description	Location(s)
272101224702	TF041-TH-CAP;0.22U ,10V ,+80-20%	C48,C531,C62,C69,C70
272101473407	TF041-TH-CAP;0.047U,10V,10%,0402	C548,C549,C550,C56,C561,C563,(
272101474703	TF041-TH-CAP; 0.47U ,CR,10V,+80-	C529,C556,C567,C569,C570,C572
272102104708	TF041-TH-CAP;0.1U ,16V,+80-20%,	C100,C103,C106,C107,C109,C118
272102223409	TF041-TH-CAP;0.022U,16V ,+-10%,0	C44,C501,C51,C521,C522,C533,C
272103103407	TF041-TH-CAP;0.01U ,CR,25V ,10%,	C632,C634,C659,C663,EC25,EC26
272105100307	TF041-TH-CAP;10P ,CR,50V ,5%,04	EC1,EC2,EC24,EC5
272105102421	TF041-TH-CAP;1000P,CR,50V,10%,04	C1,PC10,PC15,PC20,PC35,PC525
272105103704	TF041-TH-CAP;0.01U ,50V,+80-20%,	C117,C119,C122,C129,C139,C195
272105220404	TF041-TH-CAP;22P ,50V ,+ -10%,0	C629,C630,EC13,EC14,EC15,EC5
272105221410	TF041-TH-CAP;220P ,CR,50V ,10%,0	PC34
272105222503	TF041-TH-CAP;2200P,50V ,+/-20%,0	C530
272105270305	TF041-TH-CAP;27P ,50V ,5%,0402,	C651,C652
272105331303	TF041-TH-CAP;330P,CR,50V,5%,0402	PC32
272105392502	TF041-TH-CAP;3900P,50V,+/-20%,04	C642,C643,C644,C645
272105470403	TF041-TH-CAP;47P ,50V ,+ -10%,0	C95
272401227001	TF041-TH-CAP;220U,4V,EEFCX0G221Y	C179,C566,C66,C703
272430227501	TF041-TH-CAP;220uF,2V,±20%,15mo	PC550,PC572,PC580
272430337501	TF041-TH-CAP;330uF,2V,±20%,15mo	C159
272431227005	TF041-TH-CAP;220uF,6.3V,7343,25m	PC530
272431337102	TF041-TH-CAP;330U,2V,-35/+10%,H1	PC40,PC510,PC515,PC518,PC519
272431477003	TF041-TH-CAP;470U,2.5V,2R5TPE470	C36,C40
272601107521	TF041-TH-EC;100U,6.3V,+-20%,9.3*	C679,C684
272603276503	TF041-TH-EC;27uF,25V,+/-20%,H5.7	PC517,PC520
273000500184	TF041-TH-FERRITE CHIP;600OHM/100	EL19,EL20,EL23,EL35,EL36,EL3

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Part Number	Description	Location(s)
273000500267	TF041-TH-CHOKE COIL;400uH MIN,12	HL502
273000500291	TF041-TH-CHOKE COIL;0.36UH,1.1mo	PL503,PL506
273000610037	TF041-TH,FERRITE CHIP;120OHM/100	EL10,EL11,EL12,EL13,EL14,EL1
273000610041	TF041-TH,FERRITE CHIP;120OHM/100	EL540,EL541,EL543
273000501293	TF041-TH-CHOKE COIL;4.7UH,+/-30%	PL509,PL511,PL512,PL513,PL51
273000996273	TF041-TH-INDUCTOR;33uH,2.3A,93mO	PL501
273001050272	TF041-TH-TRANSFORMER;10/100 BASE	U510
274011431454	TF041-TH-XTAL;14.318MHZ,32PF,50P	X501
274012500452	TF041-TH-XTAL;25MHZ,20PF,30PPM,8	X503
274013275401	TF041-TH-XTAL;32.768KHZ,20PPM,12	X1
281307085005	TF041-TH-IC;NC7SZ08P5,2-INPUT &	U1
282574008013	TF041-TH-IC;74AHC08,QUAD 2-I/P A	U516
282574014007	TF041-TH-IC;74AHC14,HEX INVERTER	U520
282574108008	TF041-TH-IC;74AHC1G08,SINGLE AND	U501,U502
283468470002	TF041-TH-IC;EEPROM,M93C46-WMN6T,	U519
284500007017	TF041-TH-IC;ICH7M,SOUTH BRIDGE,3	U515
284500883002	TF041-TH-IC,ALC883-GR,AUDIO CODE	U518
284500945002	TF041-TH-IC;945GM,NORTH BRIDGE,3	U506
284508100015	TF041-TH-IC;RTL8100CL-LF,LAN CON	U514
284509310001	TF041-TH-IC;ICS9LPR310, LOW POWE	U505
284510321002	TF041-TH-IC;ADM1032ARZ-1,TEMPERA	U504
286100212002	TF041-TH-IC;TPA0212,AMPLIFIER,TS	U517
286300594004	TF041-TH-IC;TL594C,PWM CONTROL,S	PU2
286300692001	TF041-TH-IC;G692L293TCUf,RESET C	U4
286301117133	TF041-TH-IC;APL1117-25V,2.5V,1A,	U2

Part Number	Description	Location(s)
286302231002	TF041-TH-IC;TPS2231,POWER INTERF	U512
286306208002	TF041-TH-IC;ISL6208CBZ-T,PWM DRI	PU501,PU502
286306227003	TF041-TH-IC;ISL6227CAZ, PWM CONT	PU506
286306260002	TF041-TH-IC;ISL6260,IMVP-VI,QFN4	PU3
286388550001	TF041-TH-IC;ISL88550A,PWM,28 LD	PU508
288100032014	TF041-TH-DIODE;BAS32L,VRRM75V,ME	D505,D506,PD6
288100034012	TF041-TH-DIODE;SSA34,40V,3A,SMA	PD501,PD502,PD503,PD504
288100054034	TF041-TH-DIODE;BAT54,30V,200mA,S	D504,D507
288100054035	TF041-TH-DIODE;BAT54C,SCHOTTKY D	D1,D503
288100541004	TF041-TH-DIODE;BAT54ALT1,COM. AN	D13,D4,D7,PD506
288100701003	TF041-TH-DIODE;BAV70LT1,70V,225M	D2,D3,PD4
288101040012	TF041-TH-DIODE;PDS1040,10A SCHOT	PD5
288104148020	TF041-TH-DIODE;RLS4148,200MA,500	D501,D502
288105520002	TF041-TH-DIODE;BZV55-C20,ZENER,5	PD3
288105524005	TF041-TH-DIODE;BZV55-C2V4,ZENER,	PD7
288200114010	TF041-TH-TRANS;DTC114TKA,10K,N-M	Q15,Q16,Q527,Q528
288200144027	TF041-TH-TRANS;DDTC144WCA,NPN,SO	Q5,Q505
288200144028	TF041-TH-TRANS;DDTC144TCA,NPN,SO	Q17,Q513,Q514,Q518,Q522,Q524
288200144029	TF041-TH-TRANS;DTC144WK,NPN,SOT-	PQ501
288200144030	TF041-TH-TRANS;DDTC144TKA,N-MOSF	Q1,Q11,Q12,Q509,Q519,Q520,Q6
288200301017	TF041-TH-TRANS;FDV301N_NL,N-CHAN	Q521
288202222021	TF041-TH-TRANS;PMBT2222A,NPN,SOT	PQ9
288203413002	TF041-TH-TRANS;AO3413,P-MOSFET,S	Q10,Q14,Q4,Q507,Q510,Q515,Q5
288203414002	TF041-TH-IC;TRANS;AO3414,N-CHANN	Q3,Q511
288204403011	TF041-TH-TRANS;AO4403,P-MOSFET,4	Q504,U507,U509

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Part Number	Description	Location(s)
288204419002	TF041-TH-TRANS;AO4419,P-MOSFET,9	PQ503
288204422002	TF041-TH-TRANS;AO4422,24mOHM,N-M	PQ516,PQ520
288204433003	TF041-TH-TRANS;AO4433,P-MOS,.018	PQ7,PQ8
288204702004	TF041-TH-TRANS;AO4702, N-MOSFET,	PQ517,PU507
288204912002	TF041-TH-TRANS;AO4912,24mOHM ,SM	PQ519,PU503,PU504
288213003005	TF041-TH-TRANS;RQA130N03,N-MOSFE	PQ506,PQ508,PQ509,PQ510
288218003001	TF041-TH-TRANS;RQA180N03,N-MOSFE	PQ504,PQ505,PQ511,PQ512
288227002024	TF041-TH-TRANS;2N7002LT1,N-CHANN	PQ3,PQ4,PQ502,PQ513,PQ514,P
291000000054	TF041-TH-CON;WTB,S/T,12P,0.8MM,H	J507
291000010229	TF041-TH-CON;HDR,MA,2P*1,1.25MM,	J2
291000010327	TF041-TL-CON;HDR,MA,3P*1,1.25MM,	J502
291000000817	TF041-TH-CON;WTB,8P,1.0MM,H2.2,R	J7
291000001104	TF041-TH-CON;INVERTER,1.0mm,1A,1	J3
291000002205	TF041-TH-CON;SATA HDD,FM,15P+7P,	J510
291000002605	TF041-TH-CON;26P,1MM,H5.4,175901	J8
291000004781	TF041-TH-CON;S/T,478P,1.27MM,H4.	U503
291000011504	TF041-TH-CON;HDR,MA,15P*2,1MM,H4	J503
291000013044	TF041-TH-CON;HDR,MA,15P*2,88107-	J1
291000020001	TF041-TH-CON;HDR,1.25MM,85204-04	J10,J504
291000020227	TF041-TH-CON;HDR,MA,2P*1,1.25MM,	J9
291000012612	TF041-TL-CON;HDR,ACES,85202-2602	J4
291000151220	TF041-TH-CON;FPC/FFC,12P,0.5MM,H	J6
291000622025	TF041-TH-DIMM SOCKET;DDR2,200P,0	J508
291000622026	TF041-TH-DIMM SOCKET;DDR2,200P,0	J509
291000810003	TF041-TH-CON;PHONE JACK,2 IN 1,7	J505

Part Number	Description	Location(s)
294011200514	TF041-TH-LED;BLUE,H0.55,LTST-C19	D10,D11,D5,D8,D9
295000010207	TF041-TH-FUSE;FAST,3A,32V,1206,S	PF502
295000010213	TF041-TH-FUSE;0.14A/60V,POLY SWI	HF502
295000010214	TF041-TH-FUSE;0.5A/15V,POLY SWIT	F1
295000010218	TF041-TH-FUSE;FAST,2A,63VDC,1206	F501
295000010243	TF041-TH-FUSE;NANO,10A/125V,R451	PF501
295000010247	TF041-TH-FUSE;FAST,7A/24V,1206,S	PF503
297040100033	TF041-TH-SW;PUSH BUTTOM,5P,SPST,	SW1,SW2
331000007084	TF041-TH-CON;BATTERY,2.5mm,7A,7P	PJ501
331040050029	TF041-TH-CON;CDROM,C1240T-250A1-	J506
331710015018	TF041-TH-CON;D,FM,15P,3ROW,SUYIN	J501
342804300004	TF041-STAND OFF;MDC,M2.0 H6MM,SA	MTG501,MTG502
342804300005	TF041-STAND OFF;MINIPCI EXP,H4.3	MTG503,MTG504
481807320002	TF041-F/W ASSY;KBD CTRL,8258I-MA	U513
316807300001	TF041-TH-PCB;PWA-8258I/M BD	R01
242600000565	TF041-LABEL;BLANK,11*5MM,COMMON	
242600000562	TF041-LABEL;6*6MM,GAL,BLANK,COMM	
242600000632	TF041-LABEL;27*7MM,XF-5811;POLYI	
242600000560	TF041-LABEL;PAL,20*5MM,COMMON	
242600000566	TF041-LABEL;BLANK,7MM*7MM,PRC	
361200001024	TF041-CLEANNER;YC-336,LIQUID,STE	
361200003064	TF041-SOLDER PASTE;SN96.5/AG3.0/	
270110000015	TF041-TH-THERMISTOR;470K,5%,RA,0	PR570
270110000016	TF041-TH-THERMISTOR;10K,5%,RA,06	PR503
271125029102	TF041-TH-RES,.02,1W,1%,RL3720WT-	PR502

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Part Number	Description	Location(s)
271061474304	TF041-TH-RES;470K ,1/16W,5% ,040	R510
271061120101	TF041-TH-RES;12,1/16W,1%,0402,SM	R43,R44,R571,R572
271071751104	TF041-TH-RES;750 ,1/16W,1% ,060	PR530,PR531
271072392102	TF041-TH-RES;3.92K,1/10W,1%,0603	R24
272431227014	TF041-TH-CAP;220uF,4V,+10/-30%,2	PC555
273000610042	TF041-TH,FERRITE CHIP;220OHM/100	EL542
273000500185	TF041-TH-FERRITE CHIP;130OHM/100	EL1,EL2,EL3,EL508,EL509,EL51
273000500309	TF041-TH-CHOKE COIL;90OHM/100MHZ	EL530,EL531
274011200427	'TF041-TH-XTAL;12MHZ,16PF,30PPM,	X502
286306232002	TF041-TH-IC;ISL6232,PWM ,QSOP,28	PU505
288200144044	TF041-TH-TRANS;DDTA144WCA-F,PNP,	PQ5
294011200500	TF041-TH-LED;RED,H0.8,0603,LTST-	D6
331000016033	TF041-TH-CON;R/A,DIP TYPE,2mm,3A	PJ502
272101104442	TF041-TH-CAP;0.1U,CR,10V,10%,040	C189,C190,C191,C192
295000010219	TF041-TH-FUSE;FAST,1A,63V,1206,T	F502
271061442213	TF041-TH-RES;4.42K,1/16W,1% ,040	R697,R698
271071103117	TF041-TH-RES;10.2K,1/16W,1%,0603	PR75
271061393103	TF041-TH-RES;39K ,1/16W,1% ,0402	R726,R727
271071333102	TF041-TH-RES;33K ,1/16W,1% ,060	PR76
272103330403	TF041-TH-CAP;33P ,25V ,+/-10%,0	EC511
286303107003	TF041-TH-IC;AMS3107C,3.3V,1%,VOL	U511
272101683001	TF041-TH-CAP;0.068U,10V,0402,X7R	PC18
291000920610	TF041-TH-CON;STEREO JACK,6P,W9.5	J512,J513
342808300004	TF041-TH,FINGER;EMI GROUNDING SM	ETP3
342807300006	TF041-TH,FINGER;EMI GROUNDING SM	ETP501

Part Number	Description	Location(s)
342807300007	TF041-TH,FINGER;EMI GROUNDING SM	ETP6
481807320001	TF041-F/W ASSY;SYS/VGA BIOS,8258	U6
288100501004	TF041-TH-DIODE;ESD,PESD5V0S1BL,S	ZD3,ZD5,ZD8,ZD9
331000008145	TF041-TH-CON;SPDIF 8P,DLT13M1,MP	J514
271061204104	TF041-TH-RES;200K ,1/16W,1% ,040	PR504
291000005201	TF041-TH-CON;S/T,52P,0.8MM,H7.2,	J511
272105561302	TF041-TH-CAP;56P ,50V ,5%,0402,N	C551,C552
272105120310	TF041-TH-CAP;12P ,CR,50V ,5% ,0	C127,C128
342808300002	TF041-TH,FINGER;EMI GROUNDING SM	ETP4
339115000074	TF041-MICROPHONE;-62dB+-2dB,D6.0	MIC1
365350000004	SOLDER WIRE;LEAD_FREE,ECO,RMA98S	
242600000566	TF041-LABEL;BLANK,7MM*7MM,PRC	
622200030002	PE FILM;SKIN,PACKING,PRC	
622200000025	TAPE;SOLDER PREVENT,1/2,LL-N15A3	
340804300001	TF041-HOLDER;EXP CARD,TYCO,SABLE	
242600000564	TF041-LABEL;25*6,HI-TEMP,COMMON	
343803700001	TF041-HEATSINK;NORTHBRIDGE,8090	
346804300013	TF041-INSULATOR;CHP,SABLE GT	
346804300029	TF041-INSULATOR;SAFETY-MDC,SABLE	
346806000008	TF041-SPONGE;RTC BATTERY,8258D	
346806000023	TF041-SPONGE;MODEM PORT,8258D	
346807300001	TF041-INSULATOR;MB,TP,8258I	
346807300003	TF041-INSULATOR;SPK,SLD-MB,8258I	
346807300005	TF041-INSULATOR;MB,SOLDER,8258I	
348205015010	TF041-GASKET;2,05,015,010	

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Part Number	Description	Location(s)
348208050025	TF041-GASKET;2,08,050,025	
371102010620	TF041-SCREW;M2L6,K-HD(+1),D3.3t0	
371102010310	TF041-SCREW;M2L3,K-HD(+),D3.8,t=	
371102010521	TF041-SCREW;M2L5,BIN(+1),D4.1,t1	
343807300001	TF041-HEATSINK;SOUTHBRIDGE,8258I	
346805050001	TF041-INSULATOR;DDR SOCKET,DRAGO	
346807300006	TF041-INSULATOR;MB,CPU,8258I	
346807300007	TF041-INSULATOR;MB,MINIPCI-E,825	
348207070020	TF041-GASKET;2,07,070,020	
348208035020	TF041-GASKET;2,08,035,020	
348210010020	TF041-GASKET;2,10,010,020	
348210015020	TF041-GASKET;2,10,015,020	
422802800003	TF041-WIRE ASSY;BATT TO MB,MOLEX	J9
346807300008	TF041-INSULATOR;NEWCARD,8258I	
411807300007	TF041-PWA;PWA-8258I_8858/DD BD	
411807300009	TF041-PWA;PWA-8258I_8858/DD BD,S	
271045107104	TF041-TH-RES;.01 ,1W ,1% ,2512	AKPR502
271061101109	TF041-TH-RES;100 ,1/16W,1% ,040	AKR5,AKR7,AKR8
271061102310	TF041-TH-RES;1K ,1/16W,5% ,040	AKC502,AKC505,AKR1
271061103307	TF041-TH-RES;10K ,1/16W,5% ,040	AKR2,AKR4,AKR503,AKR505
271061104108	TF041-TH-RES;100K ,1/16W,1% ,040	AKPR504
271061105307	TF041-TH-RES;1M ,1/16W,5% ,040	AKPR506
271061151110	TF041-TH-RES;150 ,1/16W, 1%,040	AKR3,AKR6,AKR9
271061474304	TF041-TH-RES;470K ,1/16W,5% ,040	AKPR505
271071100103	TF041-TH-RES;10 ,1/16W,1% ,060	AKPR501,AKPR503

Part Number	Description	Location(s)
272001105410	TF041-TH-CAP;1U ,10%,10V ,0805	AKPC507
272073104712	TF041-TH-CAP;0.1U,25V,10%,0603,X	AKEC501
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,10%,	AKPC505
272101105705	TF041-TH-CAP;1U ,CR,6.3V ,80-2	AKC503,AKC504
272102104708	TF041-TH-CAP;0.1U ,16V,+80-20%,	AKC2,AKEC502,AKEC503
272105100307	TF041-TH-CAP;10P ,CR,50V ,5%,04	AKEC1,AKEC3,AKEC6,AKEC7,A
272105103704	TF041-TH-CAP;0.01U ,50V,+80-20%,	AKPC501
272431157520	TF041-TH-CAP;150U,KOCAP,6.3V,20%	AKC501,AKC506
273000500184	TF041-TH-FERRITE CHIP;600OHM/100	AKEL5,AKEL6
286300310001	TF041-TH-IC;SC310B,I-SENSE AMP,S	AKPU501
286309702004	TF041-TH-IC;RT9702APB,POWER DIST	AKU501,AKU502
288100024013	TF041-TH-DIODE;RLZ24B,ZENER,SOD-	AKPD501
288100701003	TF041-TH-DIODE;BAV70LT1,70V,225M	AKPD502
288204433003	TF041-TH-TRANS;AO4433,P-MOS,.018	AKPQ501
291000010229	TF041-TH-CON;HDR,MA,2P*1,1.25MM,	AKJ1
291000000713	TF041-TH-CON;MINI DIN,7P,R/A,C10	AKJ501
291000011504	TF041-TH-CON;HDR,MA,15P*2,1MM,H4	AKJ503
294011200514	TF041-TH-LED;BLUE,H0.55,LTST-C19	AKD1,AKD2
295000010247	TF041-TH-FUSE;FAST,7A/24V,1206,S	AKPF501
297040100033	TF041-TH-SW;PUSH BUTTOM,5P,SPST,	AKSW2,AKSW3
331000008134	TF041-TH-CON;R/A,4P*2,2MM,H15.64	AKJ502,AKJ504
331910000012	TF041-TH-CON;DC POWER JACK,2DC-G	AKPJ501
316807300002	TF041-TH-PCB;PWA-8258I_8858/DAUG	R01
288227002024	TF041-TH-TRANS;2N7002LT1,N-CHANN	AKPQ502
273000610041	TF041-TH,FERRITE CHIP;120OHM/100	AKEL501,AKEL502,AKEL505,AI

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Part Number	Description	Location(s)
273000500185	TF041-TH-FERRITE CHIP;130OHM/100	AKEL3,AKEL4,AKEL7
273000500309	TF041-TH-CHOKE COIL;90OHM/100MHZ	AKEL1,AKEL2,AKEL503,AKEL5
331000016032	TF041-TH-CON;V/T,DIP TYPE,2mm,3A	AKPJ502
273000610037	TF041-TH,FERRITE CHIP;120OHM/100	AKPL501,AKPL502
242600000562	TF041-LABEL;6*6MM,GAL,BLANK,COMM	
288100501004	TF041-TH-DIODE;ESD,PESD5V0S1BL,S	AKZD4,AKZD5
297140200013	TF041-TH-SW;COVER SWITCH,SPST,.1	AKSW1
346806000009	TF041-INSULATOR;SPEAKER TRB,SLD,	
346806000011	TF041-INSULATOR;TRBOARD,SOLDER,8	
346806000015	TF041-SPONGE;POWER LED,8258D	
348110010010	TF041-GASKET;1,10,010,010	
348210030010	TF041-GASKET;2,10,030,010	
340804300009	TF041-SPEAKER ASSY;L,VECO,SABLE	
340804300011	TF041-SPEAKER ASSY;R,VECO,SABLE	
340806020004	TF041-COVER ASSY;KB,8258DM	
340807320001	TF041-COVER ASSY;8258IM	
340806000005	TF041-COVER ASSY;CPU,8258D	
340806000006	TF041-COVER ASSY;HDD,8258D	
340807300001	TF041-HOUSING ASSY;8258I	
340806020001	TF041-BRACKET ASSY;TP,NORMAL,825	
342803700011	TF041-STANDOFF;IO DVI,8090	
344806020013	TF041-COVER;HINGE,R,8258DM	
344806020012	TF041-COVER;HINGE,L,8258DM	
346804300031	TF041-AL-FOIL;KB,SABLE GT	
371102010327	TF041-SCREW;M2L3,K-HD(+0),D3.7T0	

Part Number	Description	Location(s)
371102610412	TF041-SCREW;M2.6L4,K-HD(+1),D4.6	
371102610623	TF041-SCREW;M2.6L6,K-HD(+1),D4.6	
371102010269	TF041-SCREW;M2L2.5,K-HD(+0),D4T0	
370103010617	TF041-SPC-SCREW;M3L6,K-HD(+1),D5	
422806020001	TF041-CABLE FFC;TP,8258DM	
344806000026	TF041-DUMMY CARD;NEWCARD,ID2,825	
345803700008	TF041-CONDUCTIVE TAPE;INVERTER,8	
422804300023	TF041-WIRE ASSY;HW SIGNAL,MB TO	
345803700006	TF041-CONDUCTIVE TAPE;LCD,8090	
340807300002	TF041-HEATSINK ASSY;MPT,8258I	
343804300002	TF041-SPRING SCREW;HEATSINK;SABL	
413000021130	CFM Medion,TFT LCD;LP154W01-TLB5	
412806000001	TF041-PCB ASSY;D/A BD,DA-1A08-D1	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/CU0.	
411806000004	TF041-PWA;PWA-8X58 I/V BD,DA-1A0	
242804400009	TF041-TH-LABEL;BAR CODE,20*10,BL	
271071000312	TF041-TH-RES;0 ,1/16W,5% ,060	R5
271071103310	TF041-TH-RES;10K ,1/16W,5% ,060	R4
271071104108	TF041-TH-RES;100K ,1/16W,1% ,060	R8
271071105312	TF041-TH-RES;1M ,1/16W,5% ,060	R12
271071183103	TF041-TH-RES;18K ,1/16W,1% ,060	R20
271071184304	TF041-TH-RES;180K ,1/16W,5% ,060	R14
271071224305	TF041-TH-RES;220K ,1/16W,5% ,060	R21
271071303103	TF041-TH-RES;30K,1/16W,1%,0603,S	R1
271071333102	TF041-TH-RES;33K ,1/16W,1% ,060	R7

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Part Number	Description	Location(s)
271071364102	TF041-TH-RES;360K ,1/16W,1%,060	R6
271071395101	TF041-TH-RES;3.9M ,1/16W,1% ,060	R9
271071591103	TF041-TH-RES;590,1/16W,1%,0603,S	R15
271071823106	TF041-TH-RES;82K,1/16W,1%,0603,S	R2
272003105402	TF041-TH-CAP;1U ,CR,25V ,10%,0	C7
272010181303	TF041-TH-CAP;180P,2KV,5%,1206,NP	C3
272023106505	TF041-TH-CAP;10U,25V,M,1210,T2.5	C1
272030000301	TF041-TH-CAP;15P,3KV,5%,1808,NPO	C4
272071105411	TF041-TH-CAP;1U ,10V ,10%,0603,X	C13
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10%,0	C15,C8
272072224405	TF041-TH-CAP;0.22U ,16V ,10%,060	C9
272072473409	TF041-TH-CAP;0.047U,16V ,10%,060	C14
272073105404	TF041-TH-CAP;1UF ,25V,10%,0603,	C2
272073223408	TF041-TH-CAP;0.022U,CR,25V ,10%,	C16
272073332405	TF041-TH-CAP;3300P,CR,25V ,10%,0	C12
272073682404	TF041-TH-CAP;6800P,CR,25V ,10%,0	C6
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,10%,	C5
272075150308	TF041-TH-CAP;15P ,CR,50V ,5% ,0	C11
272075181308	TF041-TH-CAP;180P ,50V ,5% ,0603	C10
273001050279	TF041-TH-XFMR;CI8.5,20T/2000T,16	T1
286009910003	TF041-TH-IC;OZ9910S,CCFL CTRL ,S	U2
288100099015	TF041-TH-DIODE;BAV99,70V,450MA,S	D1,D2
288206602003	TF041-TH-TRANS;AO6602L,N&P-MOSFE	U1,U3
291000020229	TF041-TH-CON;HDR,MA,2P*1,3.5MM,R	CN2
291000021109	TF041-TH-CON;HDR,MA,11P*1,ACES,8	CN1

Part Number	Description	Location(s)
295000010397	TF041-TH-FUSE;FAST,1.5A,63VDC,12	F1
316681300005	TF041-PCB;PWA-8050 INVERTER BD,G	R0D
361200003064	TF041-SOLDER PASTE;SN96.5/AG3.0/	
340806020005	TF041-HOUSING ASSY;LCD,8258DM	
344806020007	TF041-COVER;REAR,LCD,8258DM	
344806020006	TF041-COVER;LCD,8258DM	
342806020001	TF041-BRACKET;LCD,L,8258DM	
342806020002	TF041-BRACKET;LCD,R,8258DM	
340804300002	TF041-HINGE;L,JARLLY,SABLE GT	
340804300004	TF041-HINGE;R,JARLLY,SABLE GT	
345806020001	TF041-RUBBER;COVER,LCD,8258DM	
346806020005	TF041-MYLAR;COVER,LCD,8258DM	
346802800025	TF041-INSULATOR;INVERTER,LCD,865	
371102010269	TF041-SCREW;M2L2.5,K-HD(+0),D4T0	
371102010329	TF041-SCREW;M2L3,K-HD(+0),D4T0.3	
371102610412	TF041-SCREW;M2.6L4,K-HD(+1),D4.6	
370102631204	TF041-SPC-SCREW;M2.6L6,K-HD,NIW/	
370102610807	TF041-SPC-SCREW;M2.6L8,K-HD,NIW/	
422804300003	TF041-WIRE ASSY;LCD WXGA,YI YI,S	
422804300007	TF041-WIRE ASSY;INVERTER,YI YI,S	
422806500002	TF041-WLEN ASSY;CABLE,8858I	
242664800093	TF041-LABEL;CAUTION,INVERT BD,PI	
345803700006	TF041-CONDUCTIVE TAPE;LCD,8090	
324180787522	TF041-CFM-MEDION IC,CPU;DUAL-COR	
323780340011	CFM-MEDION DDR2 SO-DIMM;HYMP564S	

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Part Number	Description	Location(s)
523402259065	TF041-CFM MEDION HDD DRIVE;HM100	
370103011402	TF041-SPC-SCREW;M3L3,NIW,K-HD(+)	
340806000013	TF041-SHIELDING ASSY;HDD,8258D	
523405320298	CFM Medion ODD DRIVE;GMA-4082N,S	
342672200010	TF041-BRACKET;CD-ROM,8500	
370102010207	TF041-SPC-SCREW;M2L2,NIW/NLK,K-H	
340806000010	TF041-BEZEL ASSY;GBS,D-SM+R9,UJ8	
346803400017	TF041-INSULATOR;BEZEL,0.6mm,8050	
346800200015	TF041-MYLAR BEZEL,POLARIS	
242670800148	TF041-LABEL;WINXP,ARTEMIS	
242803700008	TF041-LABEL;CLASS LASER,MICRO MA	
242807310001	TF041-LABEL;RATING,INVES,MEDION,	
242808300005	TF041-LABEL;BAR CODE,(25*7MM)*12	
242807310002	TF041-NAMEPLATE;INVES,MEDION,MD9	
242808300010	TF041-LABEL;25*6,HI-TEMP,COMMON,	
242807310004	TF041-CFM-MEDION;COA LABEL WIN M	
242807310003	TF041-CFM-MEDION;INTEL STICK CEN	
242803400091	TF041-LABEL;MB EOW LABEL,(18x6MM	
531080830011	TF041-KBD;88,SP,K011818Q5,8350MP	
221803440001	TF041-BOX;AK,BenQ,8050QR	
222685000001	TF041-PE BAG;ANIT-STATIC,200*350	
242300400022	TF041-LABEL;BLANK,60*80MM,LL-261	
222300820002	TF041-PE BAG;50*70MM,W/SEAL,COMM	
222804920002	TF041-PE BUBBLE BAG;200x240mm,RH	
221803450006	TF041-PARTITION;AK BOX,BenQ,8050	

Part Number	Description	Location(s)
332800002008	TF041-POWER CORD,250V2.5A 2P BL	
421311310002	TF041-CABLE ASSY;PHONE LINE,6P2C	
561867880001	SINGLE PAGE;DISPLAY ATTENTION,GN	
561580730003	TF041-MANUAL;USER'S,SP,MSN400182	
561880730001	TF041-SINGLE PAGE;WARRANTY,EN/SP	
565180732001	CFM-MEDION,MS WIN XP MCE 2005 DV	
565168680015	CFM-Medion, Nero 6.6.0 15B (w/Re	
565180732002	CFM-MEDION,SUPPORT-CD MT INVES M	
565167993012	CFM-Medion;Power Cinema Suite 2	
422803400002	TF041-CFM Medion,AC ADPT ASSY;65	
222686820002	TF041-PE BAG; L230xW310,TWO HOLE	
565167993021	CFM-MEDION;CYBERLINK POWER CINEM	
441807320006	TF041-BATT ASSY;LI-ION,11.1V/4.4	
531880730001	CFM-MEDION BLUETOOH USB ADAPTER;	
412807300003	TF041-CFM-MEDION TF041-PCB ASSY;	
222667220005	TF041-PE BAG;L560XW345,CERES	
222803410001	TF041-PROTECTING CLOTH;LCD,BenQ,	
221807320001	TF041-CARTON;INVES,MEDION,8258I	
227806000002	TF041-END CAP;NORMAL PACKING,L/R	
224802630001	TF041-PALLET;1200x1000x120MM,WHA	
221803450012	TF041-CARD BOARD;TOP/BTM,PALLET,	
221803450013	TF041-CARD BOARD;FRAME,PALLET,W/	
221803450009	TF041-PARTITION;PALLET,BenQ,8050	
242803700007	TF041-LABEL;SEAL,CARTON, § 50,MED	
221300850064	TF041-REINFORCE BRKT;L1078X50X50	

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Part Number	Description	Location(s)
221300850059	TF041-REINFORCE BRKT;L788X50X50m	
221300850051	TF041-REINFORCE BRKT;L1032X50X50	
561860000039	TF041-SINGLE PAGE;DISPLAY ATTENT	
		P/N:526280732003

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11. Reference Material

❖ Intel Yonah CPU	Intel, INC
❖ Intel 945GM North Bridge	Intel, INC
❖ Intel ICH7-M South Bridge	Intel, INC
❖ Winbond W83L951G KBC	Winbond, INC
❖ 8258I Hardware Engineering Specification	Technology Corp/MITAC
❖ Explode Views	Technology Corp/MITAC

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